RANDOM ACCESS SEMICONDUCTOR MEMORIES

MODULE OUTLINE

1. BASIC MEMORY CONCEPTS
2. STATIC READ WRITE MEMORY, SRAM
3. DYNAMIC RANDOM ACCESS MEMORY, DRAM
4. ADVANCED MEMORY TECHNOLOGIES
5. ERASABLE PROGRAMMABLE READ-ONLY MEMORY, EPROM
6. MEMORY SYSTEM DESIGN
7. MEMORY CLASSES

RAM vs. ROM

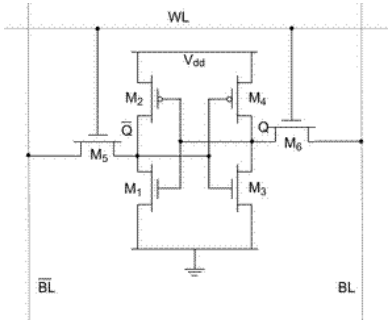
- Volatile
- RAM (random access)
  - SRAM (static)
    - Synchronous
    - Asynchronous
  - DRAM (dynamic)
    - FPM DRAM
    - EDO DRAM
    - SDRAM
    - DDR SDRAM
    - DDR2 SDRAM
    - Etc..

- Non-volatile
- ROM (read only)
  - System/Video BIOS
- PROM
  - OTP with fuses/anti-fuses
- EPROM
  - UV light for erasure
- EEPROM
  - Reprogrammable with software and hardware

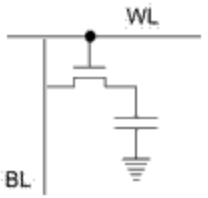
  ↳Flash Memory

SRAM & DRAM

- SRAM
  - Pros
    - Extremely Fast
    - No refresh cycle
  - Cons
    - Large area - 6T/bit
    - Expensive
  - Applications
    - Memory caches L1 & L2



- DRAM
  - Pros
    - Cheaper
    - Higher density - 1T/bit
  - Cons
    - Slower in speed
    - Needs refresh cycle
  - Applications
    - Computer memory



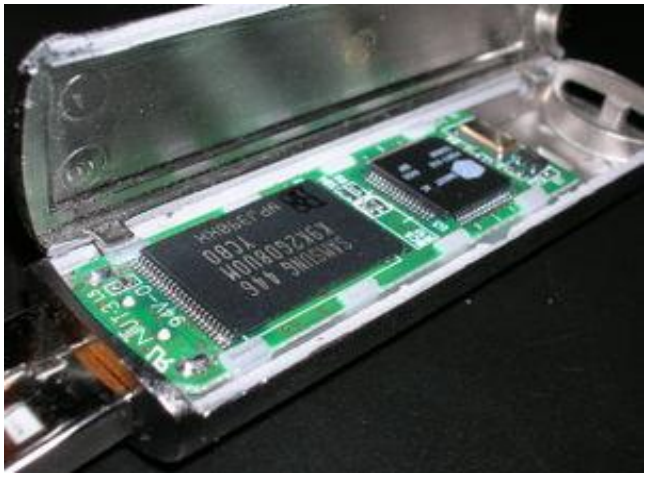
Flash Memory

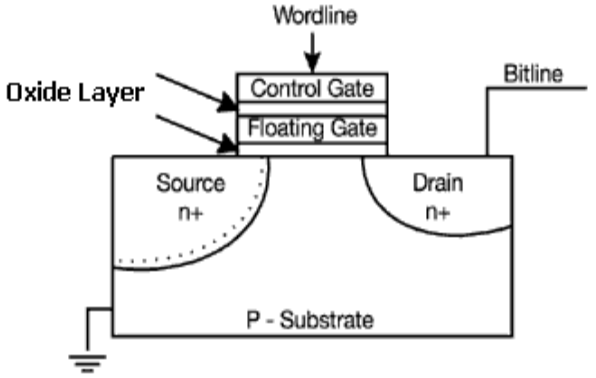
Pros

- Non-volatile
- Portability
- High Density
  - Floating gate transistor
    - CG and FG
    - MLC technology
- High Isolation

Cons

- Oxide layers near min. limit
- High voltage required
- Slow WRITE cycle
- Capacitance Coupling
- Limited Use



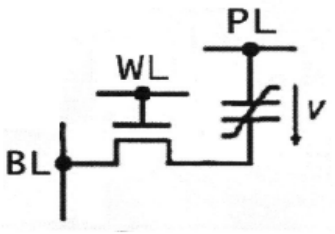


Focus For Improvement

- Non-volatility
- Portability
- Small Area
- High Density
- Faster WRITE/ERASE cycles
- Lower Power
- Lower Costs
- Longevity

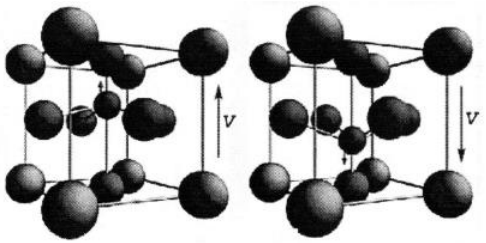
FRAM

- FeRAM (Ferroelectric RAM)
  - Uses ferroelectric characteristics of the capacitor
    - lead (Pb) zirconate (Zr) titanate (Ti) - PZT



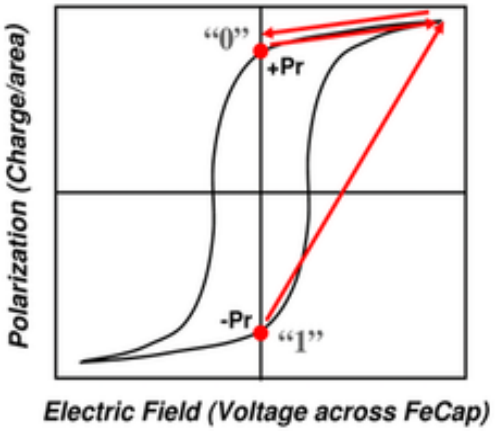
Pros

- Non-volatile
- Small size
- Fast WRITE cycles



Cons

- A potential WRITE after each READ
- Longevity
- Polarization degradation
- Requires high temperatures
- Want higher densities



MRAM

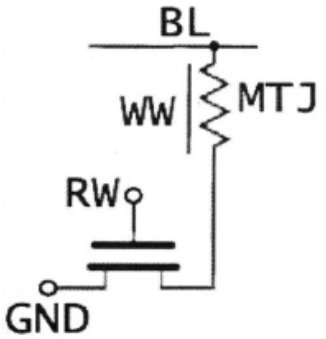
- Magnetoresistive RAM
  - Uses properties of magnetism and the development of the MTJ
  - Uses STT technology (Spin Torque Transfer)

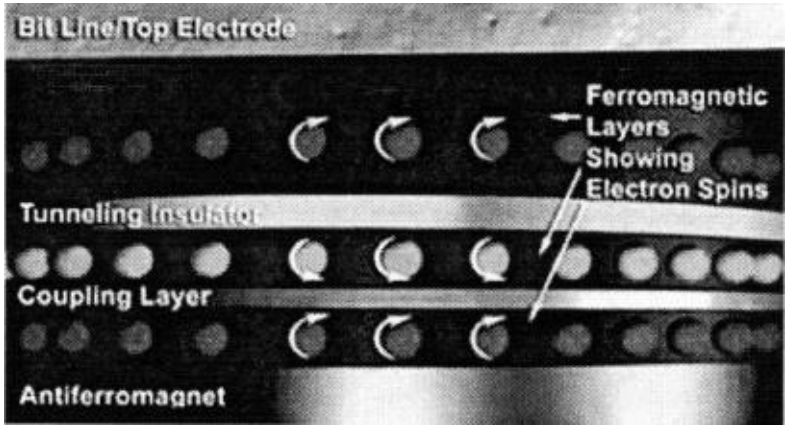
Pros

- Non-volatile
- Small size
- Fast WRITE cycles
- Longevity

Cons

- Requires high temperatures
- Want higher densities





PRAM

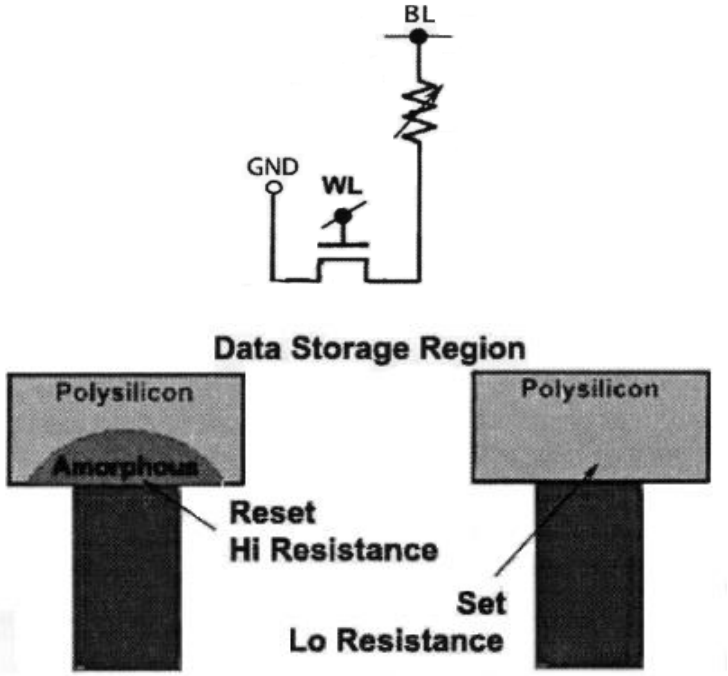
- Phase-change RAM, PCM, C-RAM (chalcogenide RAM)
  - Uses the special property of chalcogenide alloy
    - Germanium (Ge), antimony (Sb) and tellurium (Te) – GST
    - Switches between amorphous (0) and crystallized (1) states with heat from current

Pros

- Non-volatile
- Small size
- High density
- Fast switching times

Cons

- Requires high current (heat)
- Longevity



Comparisons

- Overall View

Parameters	SRAM	DRAM	Flash	FRAM	MRAM	PRAM
Non-volatile	No	No	Yes	Yes	Yes	Yes
Refresh	No	ms	No	No	No	No
Cell Size	6T	1T1C	1T	1T1C	1TCMTJ	1T1R
Read Time	2 ns	10 ns	70ns	10ns	10ns	10ns
Write Time	2 ns	10 ns	10μs	20 ns	5 ns	5 ns
Write cycles	$> 10^{15}$	$> 10^{15}$	10^{5}	$> 10^{12}$	$> 10^{15}$	$> 10^{12}$

2.1. BASIC MEMORY CONCCEPTS

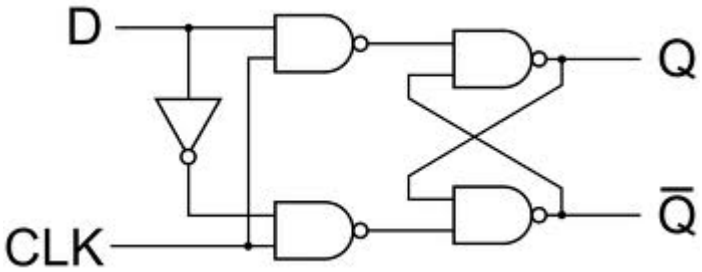
2.1.1. FLIP-FLOP / 1-BIT REGISTER

- **Smallest unit of information is a bit (0 or 1)**
- **Can be stored in a Flip-Flop (ON or OFF)**
- **Common: D-type Flip-Flop, a bistable sub-system or device**

2.1. BASIC MEMORY CONCCEPTS

2.1.1. FLIP-FLOP / 1-BIT REGISTER - contnd

- **Positive clock pulse (0 to 1):**
  - **Leading or Rising edge**
  - **Positive transition**
- **Negative clock pulse (1 to 0):**
  - **Trailing or Falling edge**
  - **Negative transition**



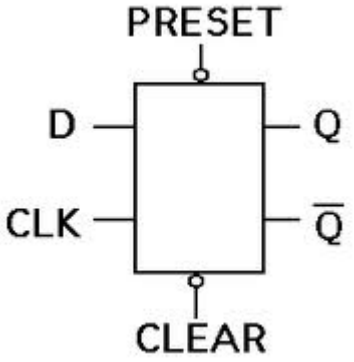


Figure 1: D-type Flip-Flop: (a) Logical diagram; (b) IC Cicuitry

2.1. BASIC MEMORY CONCCEPTS

2.1.1. FLIP-FLOP / 1-BIT REGISTER - contnd

- **Level triggered Flip-Flop: LATCH**
  - **When clock is 1 – Flip-Flop changes its state**
  - **When clock transitions (1 to 0)**
  - **The data present at D input is latched (transferred)**

Figure 1: D-type Flip-Flop: (a) Logical diagram; (b) IC Cicuitry

2.1. BASIC MEMORY CONCCEPTS

2.1.2. m-BIT REGISTERS

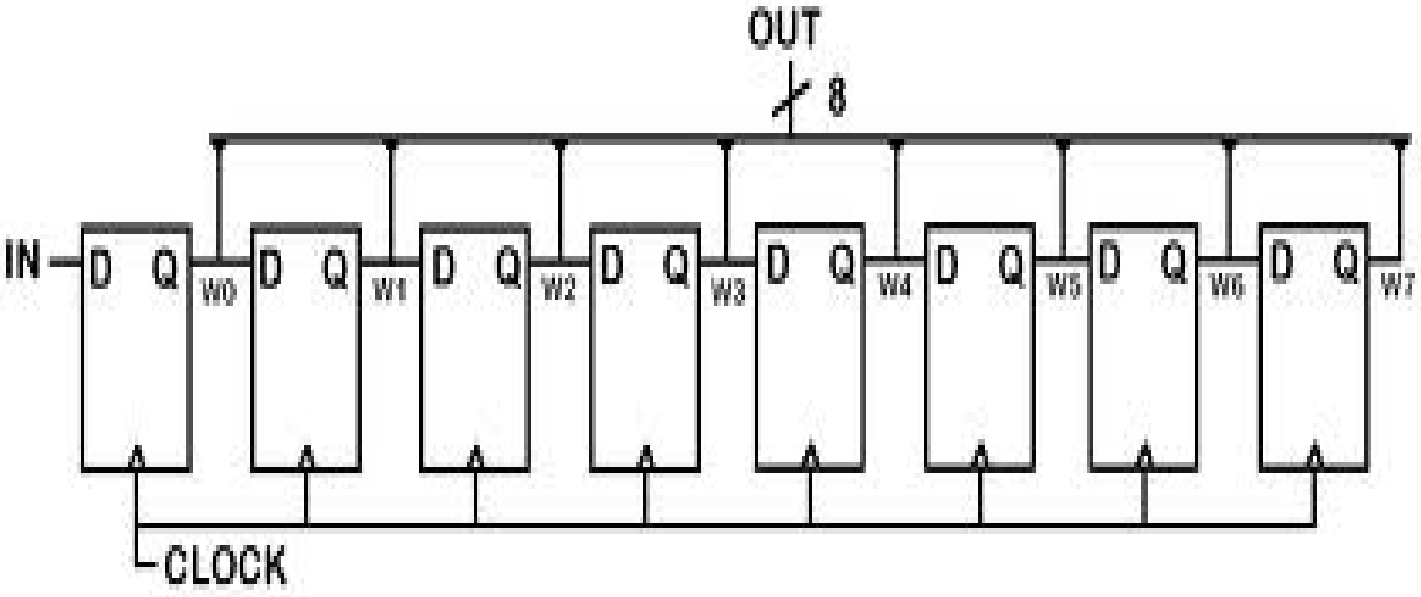


Figure 2: 8-bit (Octal) Register

2.1. BASIC MEMORY CONCCEPTS

2.1.2. m-BIT REGISTERS - contd

- **The m bits make a Word**
- **m is known as a Word length**
- **In digital systems, the Word length is 8 bits = Byte**
- **Half of a byte is known as Nibble**
- **Three-state buffers are buffers (registers) with three output states (0, 1 and undetermined)**

2.1. BASIC MEMORY CONCCEPTS

2.1.3. DATA TRANSFERS BETWEEN REGISTERS

- **Source registers on one side**
- **Destination registers on the other**
- **Data bus between registers – UNIDIRECTIONAL (?)**
- **Data contention (may lead to data corruption)**
- **Common Input to Output registers = DIRECTIONAL Data bus**
- **The memory capacity is measured in bits, byte and its multiple (kB, MB, GB, …)**

2.2. STATIC READ WRITE MEMEORY, SRAM

2.2.1. EXTERNAL ORGANISATION

- **Typical SRAM are of 1, 4 or 8 bits Word Lengths**
- **Pins on a RWM: Address, Data, Control, Power, GND and Clock.**
- **Common I/O often used**

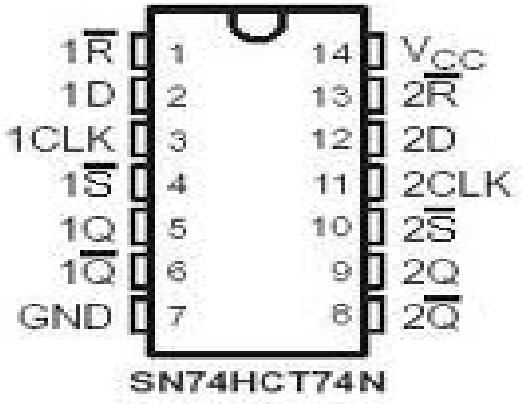


Figure 3: Memory chip

2.2. STATIC READ WRITE MEMEORY, SRAM

2.2.2. INTERNAL ORGANISATION

- **Array of memory cells (1 bit)**
- **Logic to address any memory location.**
- **Circuitry to read content of any address**
- **Circuitry to write to any memory address**
- **Logic circuitries make up logical Word**
- **Physical Word – number of bits**

2.2. STATIC READ WRITE MEMEORY, SRAM

2.2.3. TIMING REQUIREMENTS

A. STEPS FOR MEMORY READ

- Address applied to input.
- SRAM is selected by CS input
- Selected content appears at the output => Access time
- Logic circuitries make up logical Word
- Physical Word – number of bits

2.2. STATIC READ WRITE MEMEORY, SRAM

2.2.3. TIMING REQUIREMENTS

B. STEPS FOR MEMORY WRITE

- **Address applied to input.**
- **SRAM is enabled by logic level of CS input**
- **Input takes data to be written**
- **Write Enable (WE) goes low**
- **Address and CS signals are reallocated**

2.6. COMPUTATION OF TIMING REQUIREMENTS FOR MEMORY

- **READ OPERATION**

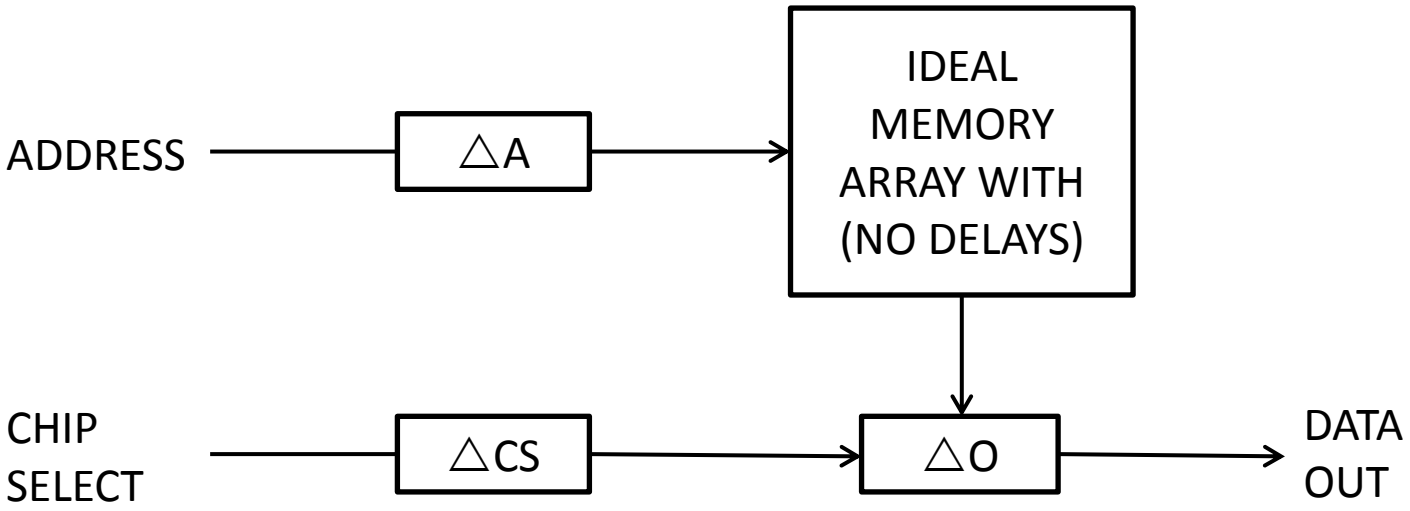


Figure 2.6.1: Lumped delay memory model for a read operation

2.6. COMPUTATION OF TIMING REQUIREMENTS FOR MEMORY

- **READ OPERATION – contd**
  - **Figure 2.6.1 depicts a model of an ideal SRAM (with no delays in signal propagation for a read operation).**
  - **In a real device, there are delays:**
    - **Two input delays: △A and △CS**
    - **One output delay: △O**
  - **Total delay from address application to output is △A + △O**
  - **Total delay from chip select signal to output is △CS + △O**
  - **Let's see timing constraints in the hand-drawn diagram.**

2.6. COMPUTATION OF TIMING REQUIREMENTS FOR MEMORY

- **READ OPERATION – contd**
  - **t_A: Access Time, it's the time elapsed from the subsequent application of an address at the Address Inputs to the appearance at the memory's output of a stable copy of the Address data.**
  - **t_{CO} : Chip Select to Output (Data) valid.**
  - **t_{DF}: Chip Deselect to output Float transition)Time**
  - **t_{OH}: Output Hold from Address change, it's maximum period of previous output data is valid after the address is changed.**
  - **t_{RC}: Read Cycle Time, it specifies the maximum rate at which at which different memory locations can be successfully read.**

2.6. COMPUTATION OF TIMING REQUIREMENTS FOR MEMORY

- **WRITE OPERATION**

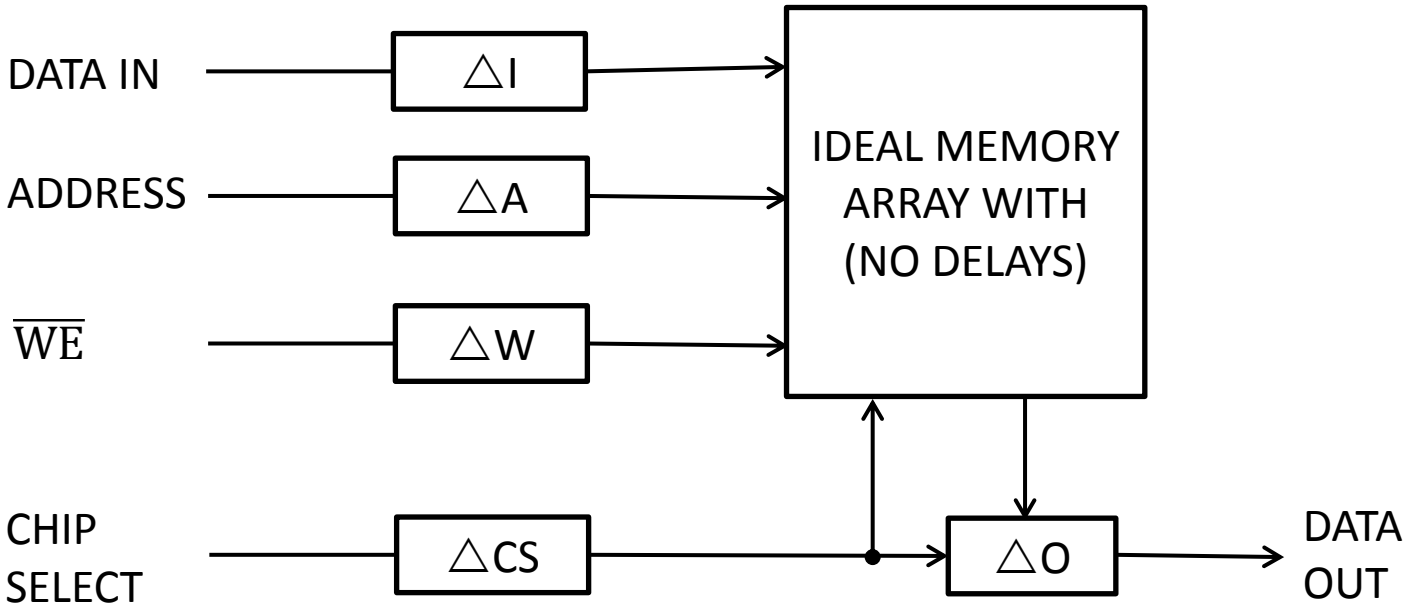


Figure 2.6.2: Lumped delay memory model for a write operation

2.6. COMPUTATION OF TIMING REQUIREMENTS FOR MEMORY

- **WRITE OPERATION – contd**
  - **Figure 2.6.2 depicts a model of an ideal SRAM (with no delays in signal propagation for a write operation).**
  - **In a real device, there are delays:**
    - **Four input delays: △I, △A, △W and △CS**
    - **One output delay: △O**
  - **Number of considerations are in play for a successful write operation**
  - **Delay in changes in input data at the package input pins is given by △I.**
  - **Data stable at the package input pins at least △I - △W earlier.**
  - **For more details on timing constraints, let's see the following hand-drawn digram…**

2.6. COMPUTATION OF TIMING REQUIREMENTS FOR MEMORY

- **READ OPERATION – contd**
  - **t_{AW}: Write delay, indicates how long the address must be stable before the write pulse changes from 1 to 0.**
  - **t_{CW} : Chip Enable to Write Time, indicates how Chip Select stable period before $\overline{WE}$ line changes from 0 to 1.**
  - **t_{DH}: Data Hold from write time, it's the period during the input data is held stable after the $\overline{WE}$ line changes from 0 to 1.**
  - **t_{DW}: Data to Write Time overlap, it's data setup time; this is the period during which data is stabe.**
  - **t_{WCY}: Write Cycle Time, it specifies the minimum time between write operations.**
  - **t_{WP}: Write Pulse Time, it's minimum length of time to guarantee writing into the slowest memory devices.**
  - **t_{WR}: Period during which the address must be held stable after the 0 to 1 transition of $\overline{WE}$.**

2.7. ERASABLE PROGRAMMABLE READ-ONLY MEMORY, EPROM

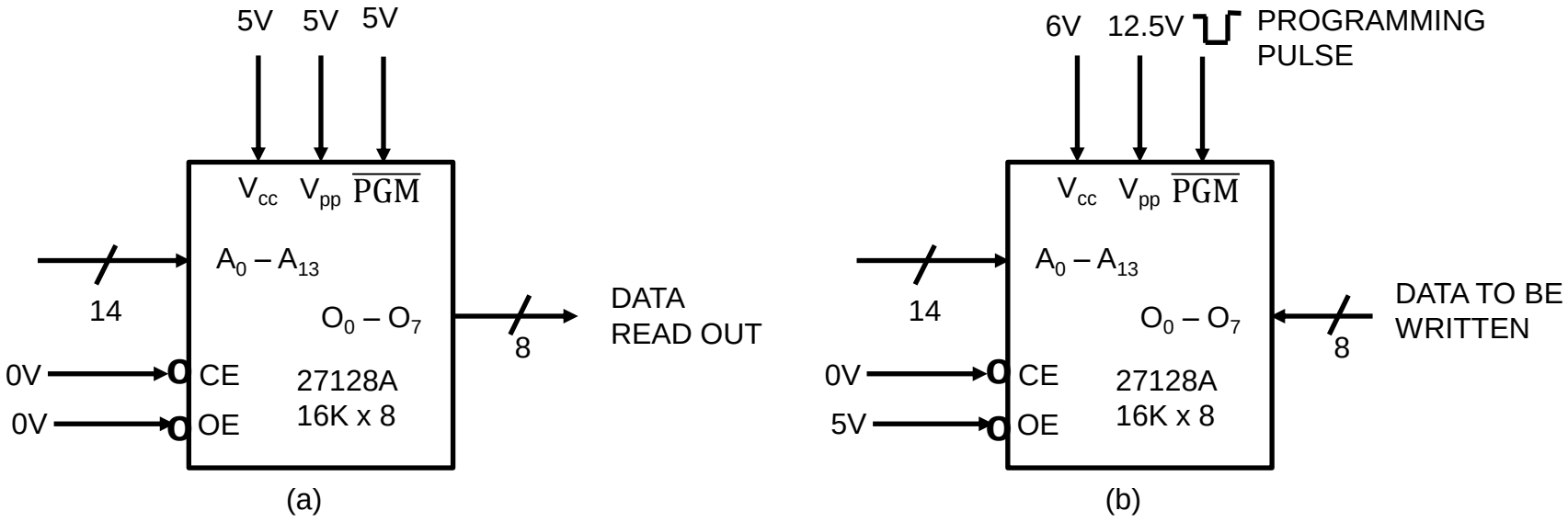
2.7.1. INTRODUCTION

- **EPROM is made by use of ultraviolet light.**
- **EPROM is non-volatile.**
- **Erasure is done by shining ultraviolet light**
- **Must remove EPROM from the microprocessor system before writing o it.**
- **EPROM programmer is special instrument for programming EPPROM chips.**

2.7. ERASABLE PROGRAMMABLE READ-ONLY MEMORY, EPROM

2.7.2. ORGANISATION AND IN-CIRCUIT OPERATION - EPROM's external organisation is similar to SRAM, except there is no $\overline{WE}$.

Figure 27.2.1: 27128A EPROM External connections: (a) Configuration for in-circuit read operation; (b) Configuration for programming on an EPROM programmer



2.7. ERASABLE PROGRAMMABLE READ-ONLY MEMORY, EPROM

2.7.3. EPROM PROGRAMMERS AND INTELLIGENT PROGRAMMERS

- **Generic device programmers.**
- **Two types by their operation mode:**
  - **Standalone programmer**
  - **PC-driven programmer**
- **Microprocessor are critical in programming EPROM.**
- **Intelligent programmers use intelligent algorithms with short pulses.**

2.8. MEMEORY SYSTEM DESIGN

1. **Estimate RAM and ROM required**
2. **Determine address boundaries**
3. **Select memory devices**
4. **Determine layout to achieve Word lengths**
5. **Draw detailed memory mapping**
6. **Determine buffering requirement**
7. **Determine memory access speed**

2.8. PRACTICAL MEMORY DESIGN

2.8.1. TYPES OF MEMORY DECODING

– Exhaustive Decoding:

- **All address bits are decoded for selection of a memory location**
- **Leads to one-to-one mapping of addresses and memory locations**
- **Also referred to as *fully decoded* memory.**

– Partial Decoding:

- **Not all addresses bits are decoded**
- **Results in simplified decoding logic**
- **Leads to many-to-one mapping of addresses to memory locations.**

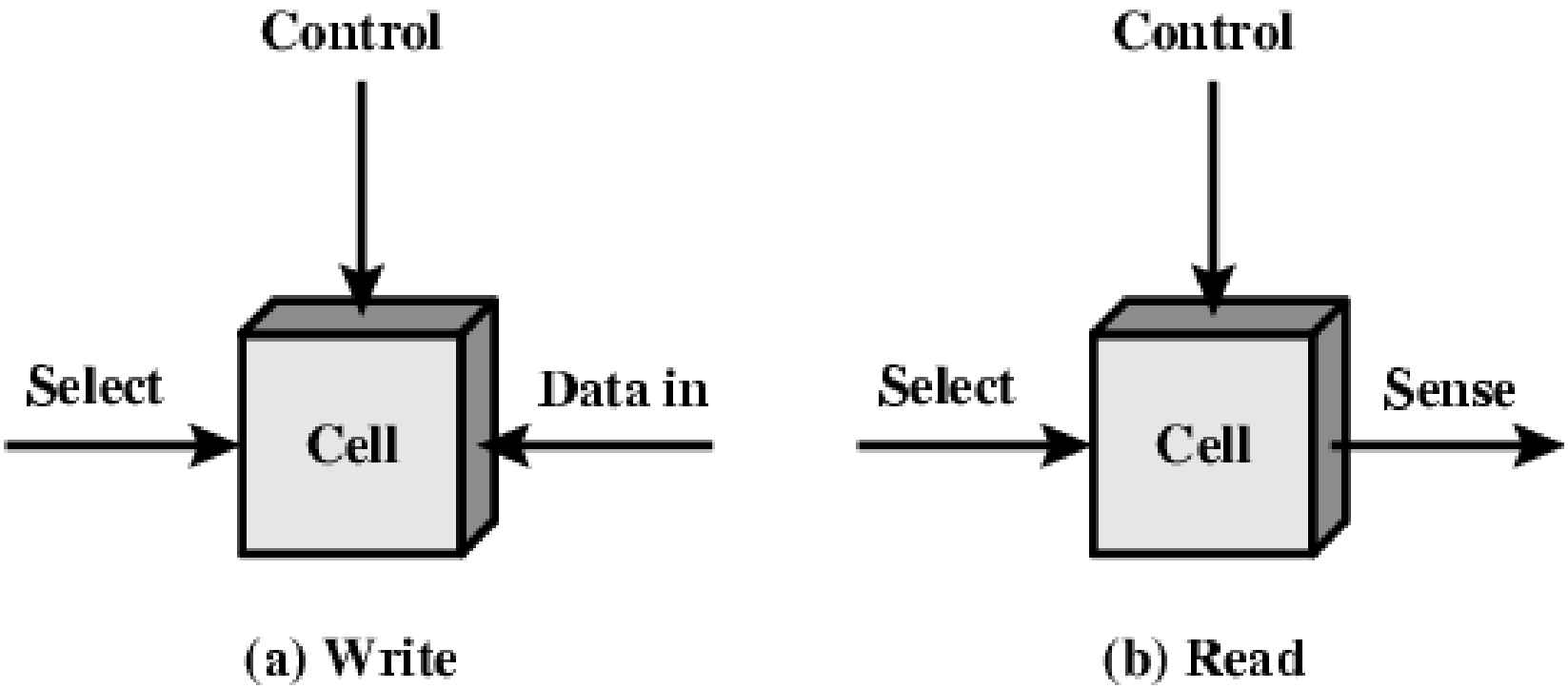
Semiconductor Memory

- RAM
  - Misnamed as all semiconductor memory is random access
  - Read/Write
  - Volatile (contents are lost when power switched off)
  - Temporary storage
  - Static or dynamic
    - Dynamic is based on capacitors – leaks thus needs refresh
    - Static is based on flip-flops – no leaks, does not need refresh

Semiconductor Memory Types

Memory Type	Category	Erasure	Write Mechanism	Volatility
Random-access memory (RAM)	Read-write memory	Electrically, byte-level	Electrically	Volatile
Read-only memory (ROM)	Read-only memory	Not possible	Masks	Nonvolatile
Programmable ROM (PROM)			Electrically	
Erasable PROM (EPROM)	Read-mostly memory	UV light, chip-level		
Electrically Erasable PROM (EEPROM)		Electrically, byte-level		
Flash memory		Electrically, block-level		

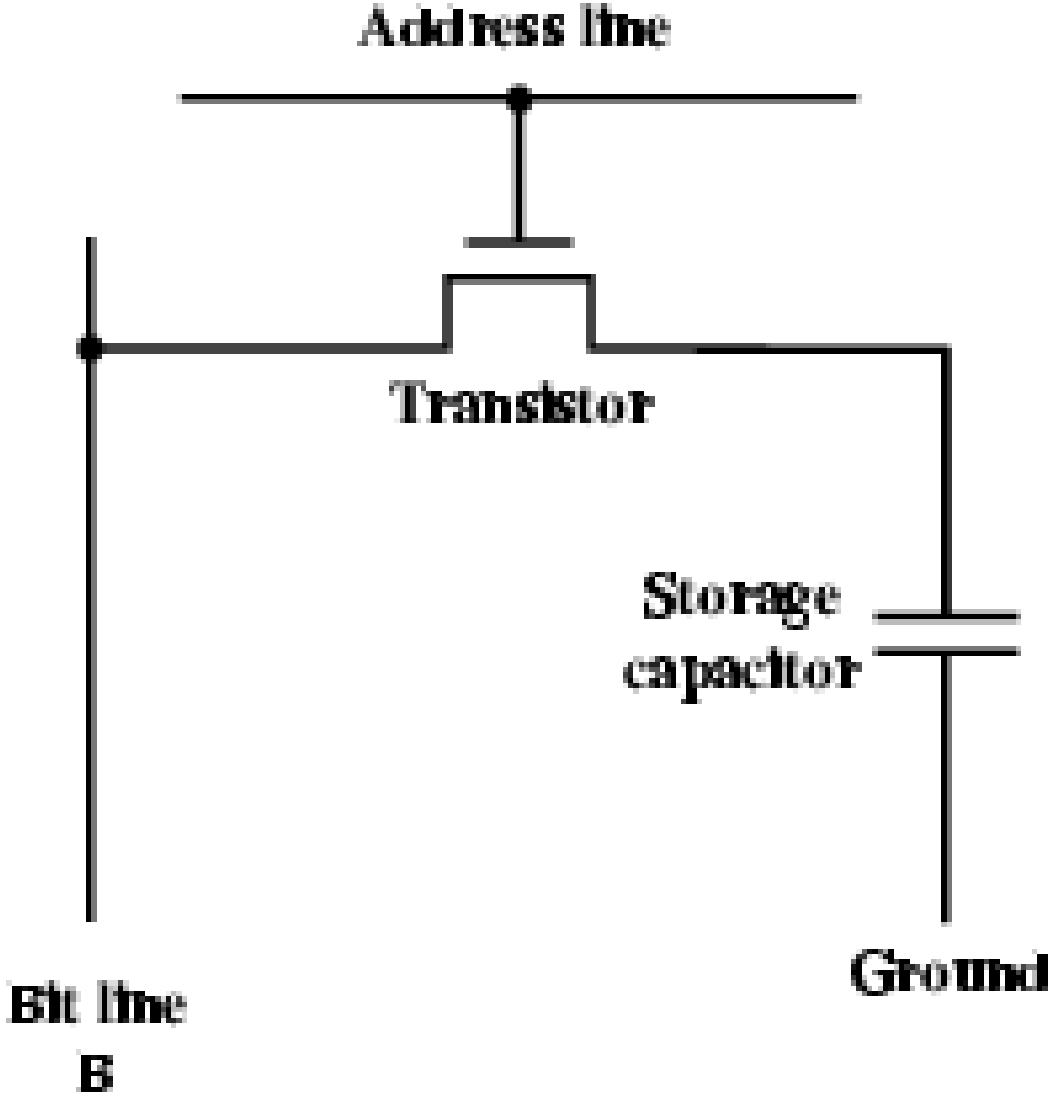
Memory Cell Operation



Dynamic RAM

- Bits stored as charge in capacitors
- Charges leak
- Need refreshing even when powered
- Simpler construction
- Smaller per bit
- Less expensive
- Need refresh circuits
- Slower
- Used in main memory
- Essentially analogue
  - Level of charge determines value

Dynamic RAM Structure



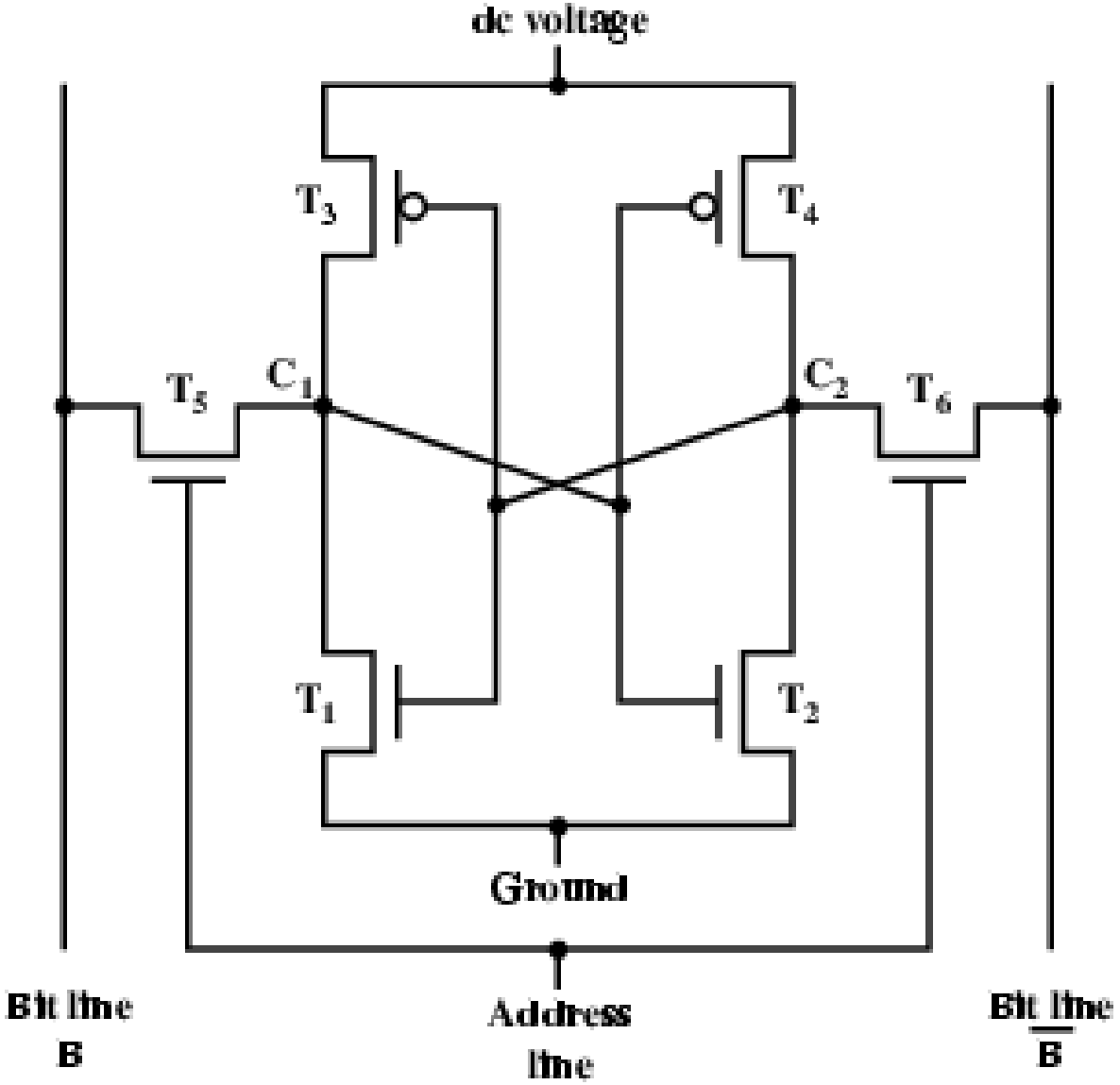
DRAM Operation

- Address line active when bit read or written
  - Transistor switch closed (current flows)
- Write
  - Voltage to bit line
    - High for 1 low for 0
  - Then signal address line
    - Transfers charge to capacitor
- Read
  - Address line selected
    - transistor turns on
  - Charge from capacitor fed via bit line to sense amplifier
    - Compares with reference value to determine 0 or 1
  - Capacitor charge must be restored

Static RAM

- Bits stored as on/off switches
- No charges to leak
- No refreshing needed when powered
- More complex construction
- Larger per bit
- More expensive
- Does not need refresh circuits
- Faster
- Cache
- Digital
  - Uses flip-flops

Static RAM Structure



Static RAM Operation

- Transistor arrangement gives stable logic state
- State 1
  - C_1 high, C_2 low
  - T_1 T_4 off, T_2 T_3 on
- State 0
  - C_2 high, C_1 low
  - T_2 T_3 off, T_1 T_4 on
- Address line transistors T_5 T_6 is switch
- Write – apply value to B & compliment to $\overline{B}$
- Read – value is on line B

SRAM v DRAM

- Both volatile
  - Power needed to preserve data
- Dynamic cell
  - Simpler to build, smaller
  - More dense
  - Less expensive
  - Needs refresh
  - Larger memory units
- Static
  - Faster
  - Doesn’t need refresh
  - Cache
  - Consumes more power

Read Only Memory (ROM)

- Permanent storage
  - Nonvolatile
- Microprogramming (see later)
- Library subroutines
- Systems programs (BIOS)
- Function tables

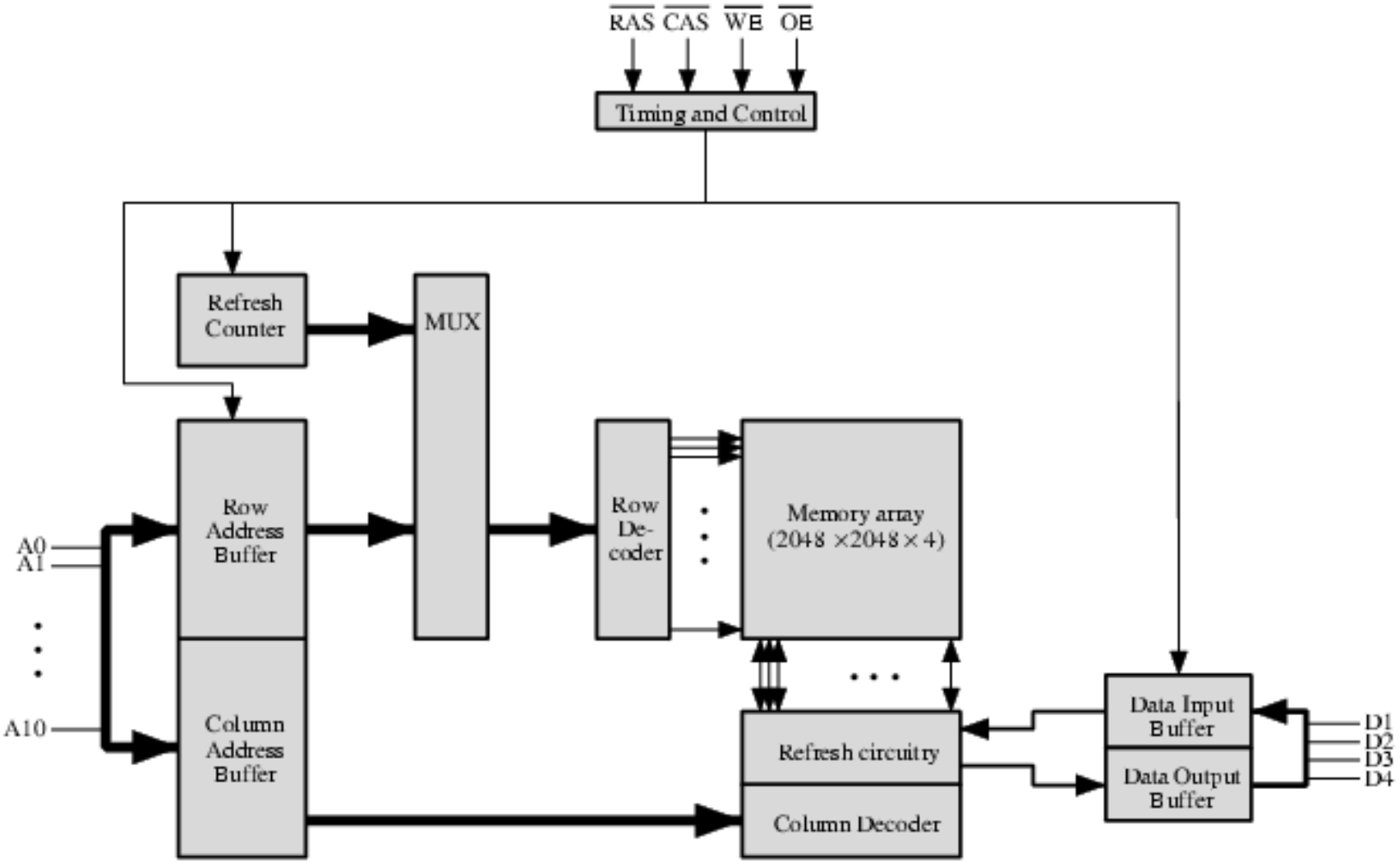
Types of ROM

- Written during manufacture
  - Very expensive for small runs
- Programmable (once)
  - PROM
  - Needs special equipment to program
- Read “mostly”
  - Erasable Programmable (EPROM)
    - Erased by UV
  - Electrically Erasable (EEPROM)
    - Takes much longer to write than read
  - Flash memory
    - Erase whole memory electrically, no byte-level erase
    - But much faster write

Memory Organization Designs

- Physical arrangement is same as logical
  - A 16Mbit chip is organized as 1M of 16 bit words
- One bit per chip system
  - 16 instances of 1Mbit chips, with bit 1 of each word in chip 1 and so on
- A 16Mbit chip can be organised as a 2048 x 2048 x 4bit array
  - $16M = 2^{24} = 2^{11} * 2^{11} * 4$
  - Reduces number of address pins
    - Multiplex row address and column address
    - 11 pins to address (2^{11}=2048)
    - Adding one more pin doubles range of values so x4 capacity (because each dimension of the square array is doubled)

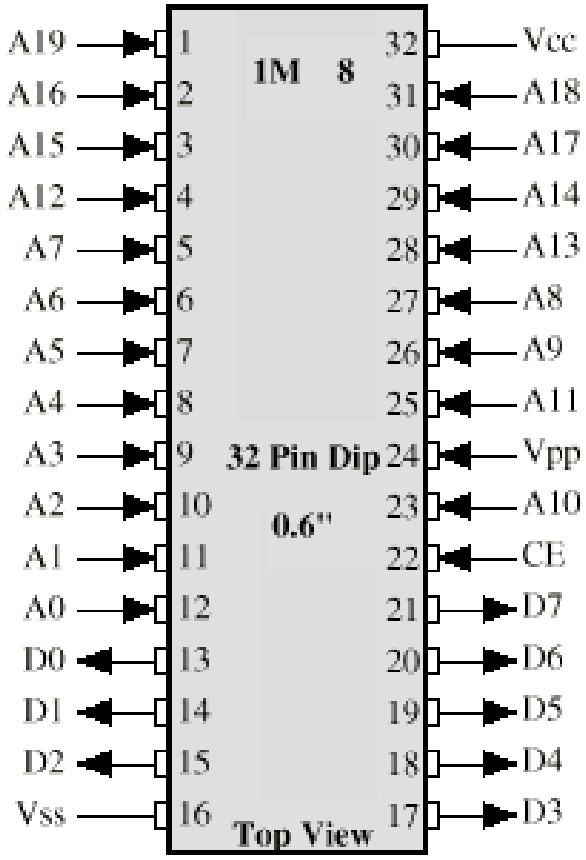
Typical 16 Mb DRAM (4M x 4)



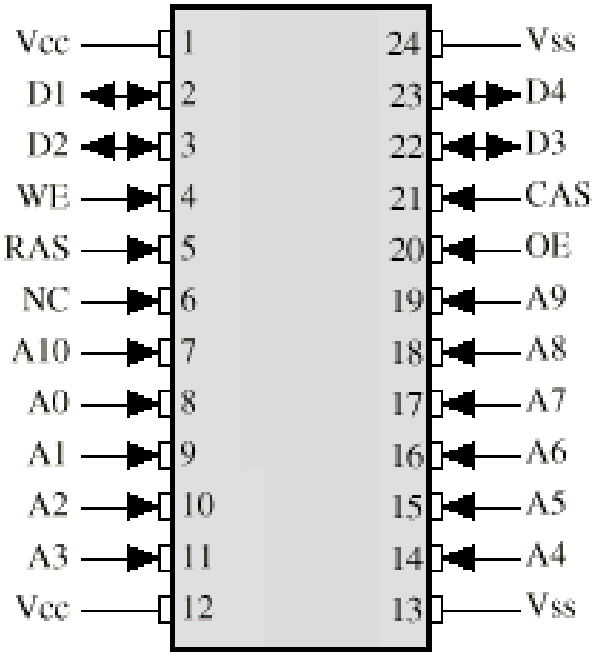
Refreshing

- Refresh circuit included on chip
- Disable chip while refreshing
- Refresh row by row
- Read & Write back
- Takes time
- Slows down apparent performance

Packaging



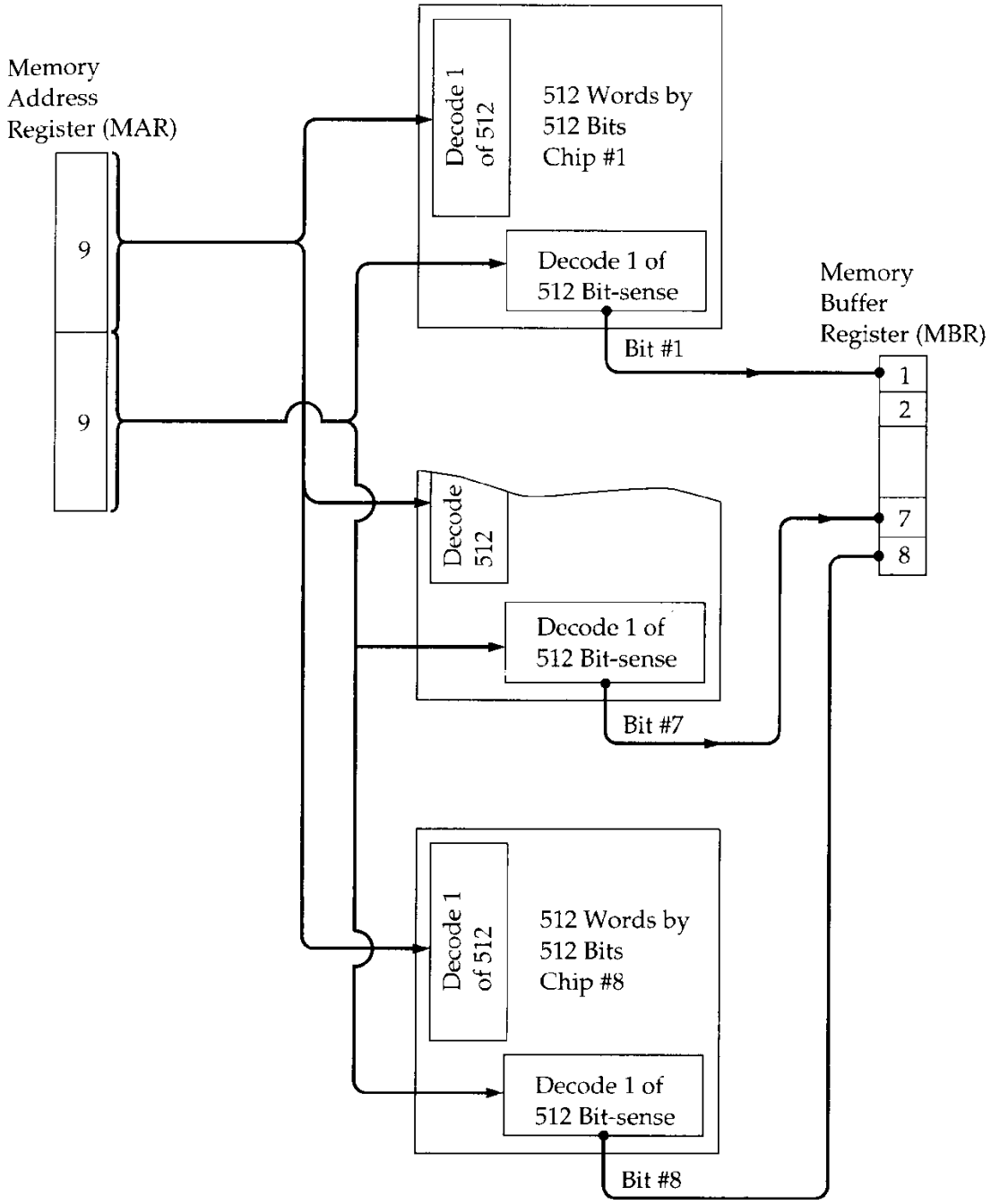
(a) 8 Mbit EPROM



(b) 16 Mbit DRAM

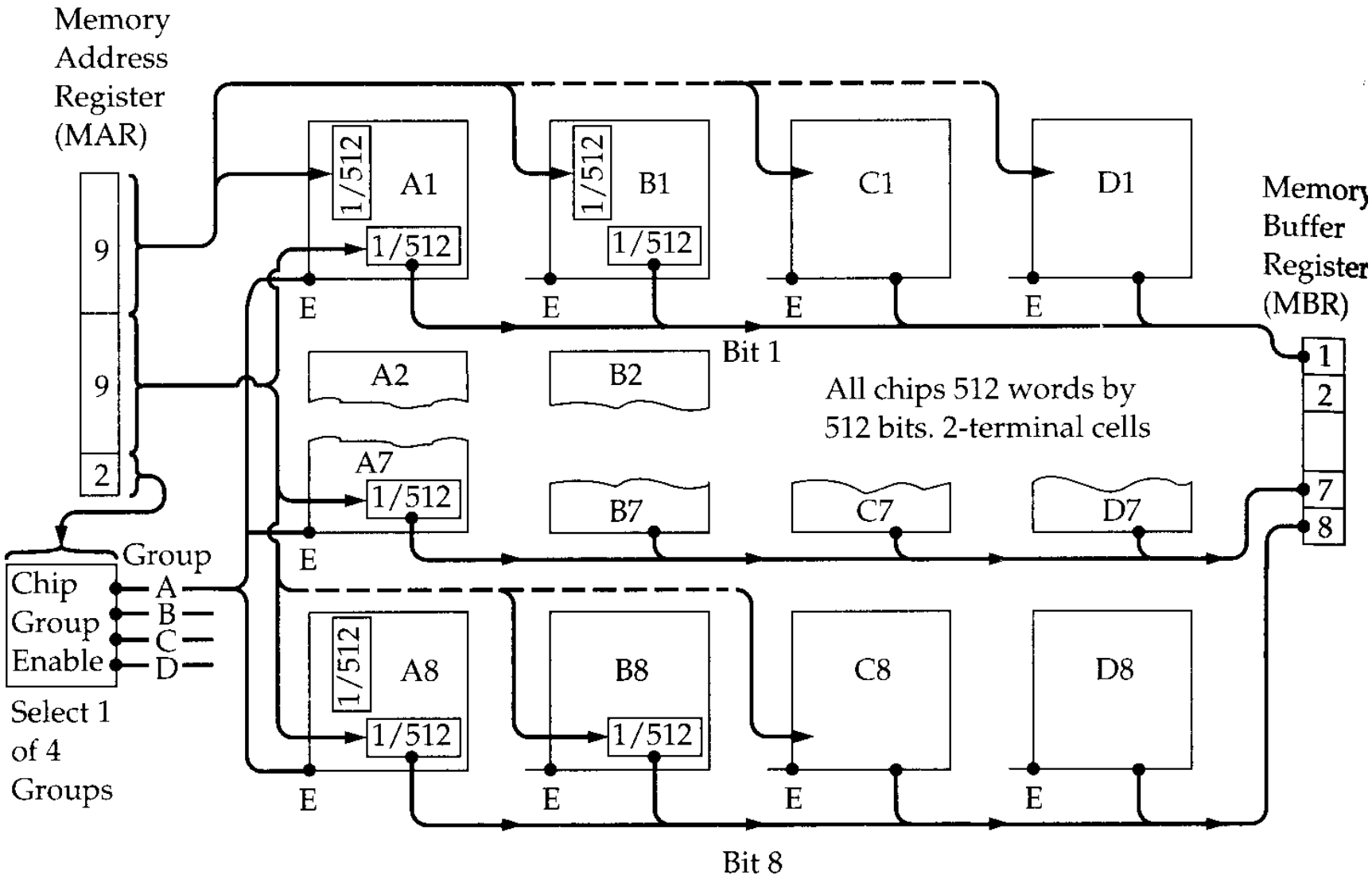
Or

- Multiple chips make up the entire memory
- 1 bit per chip system org.
- 8 256K x 1 bit chips



Module Organization

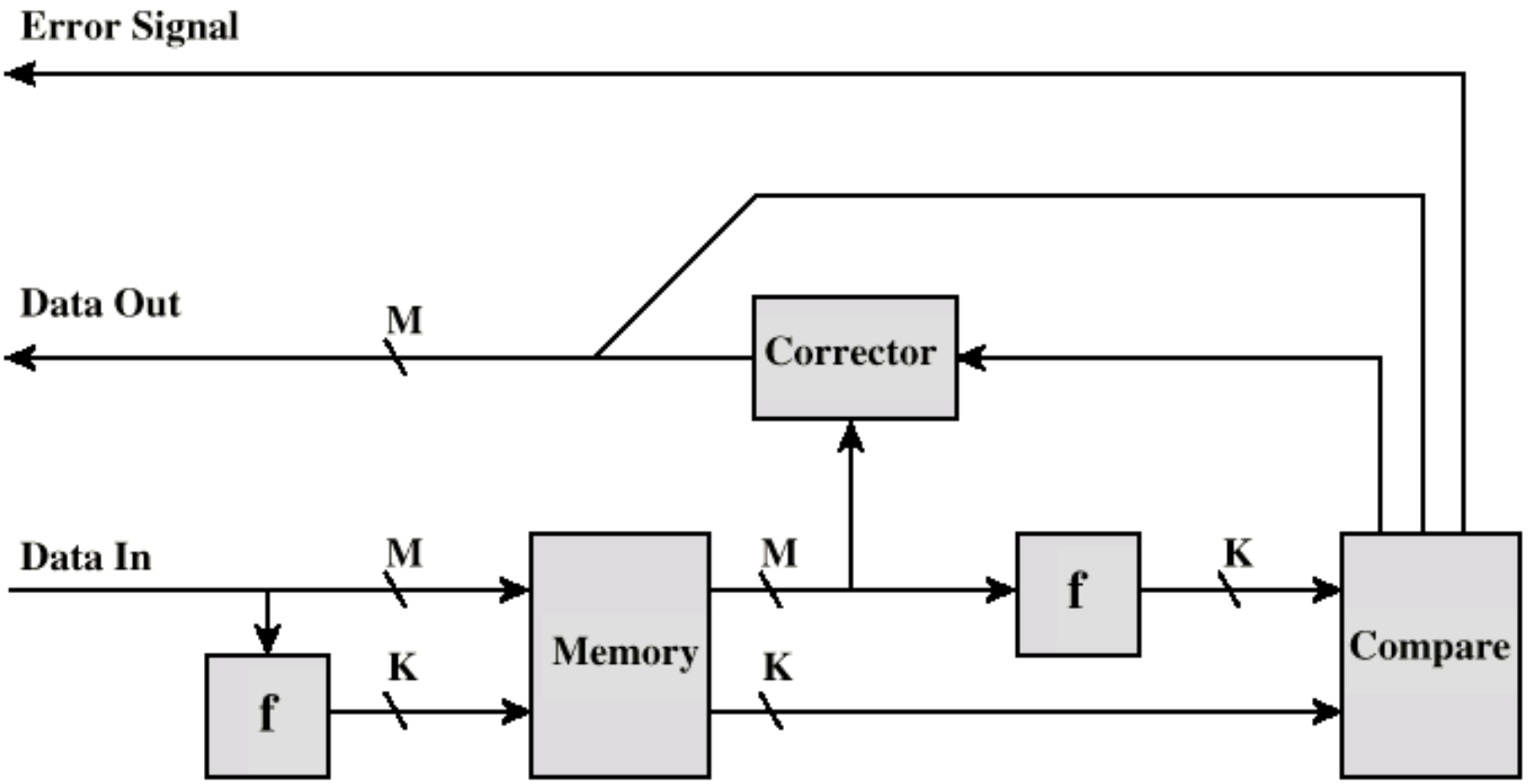
- 1 M 8 bit words



Error Correction

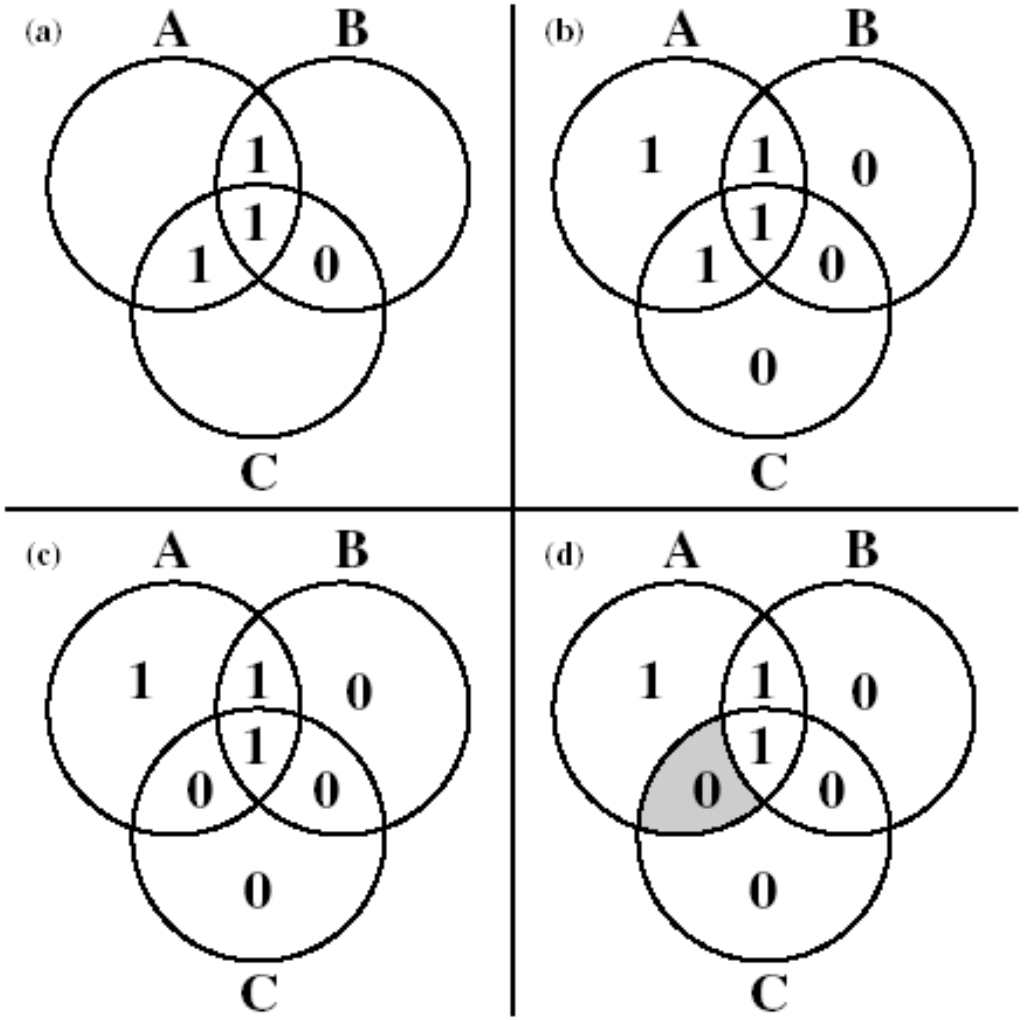
- Hard Failure
  - Permanent defect
- Soft Error
  - Random, non-destructive
  - No permanent damage to memory
  - E.g. alpha particles from radioactive decay
  - Present in all materials
- Detected using Hamming code
- Can be also repaired using error correcting code
- SEC-DED code: single error correcting - double error detecting code
  - can detect 2 errors, can correct 1

Error Correcting Code Function



Hamming Code Operation

- Parity bits can detect error



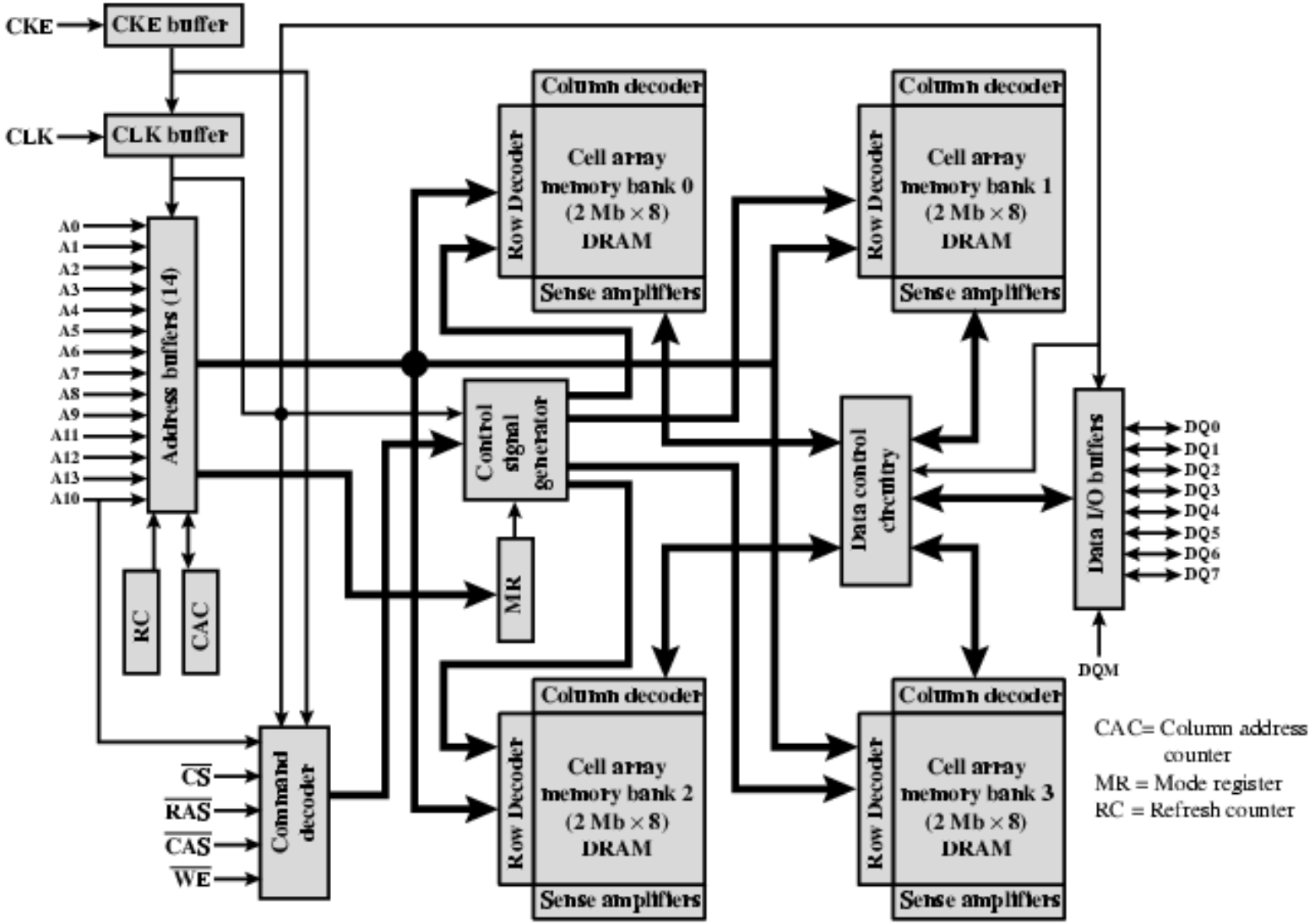
Advanced DRAM Organization

- Basic DRAM same since first RAM chips
- Enhanced DRAM
  - Contains small SRAM as well
  - SRAM holds last line read (locality of reference)
- Cache DRAM
  - Larger SRAM component
  - Used as cache or serial buffer

Synchronous DRAM (SDRAM)

- Access is synchronized with an external clock
- Address is presented to RAM
- RAM finds data (CPU waits in conventional DRAM)
- Since SDRAM moves data in time with system clock, CPU knows when data will be ready
- CPU does not have to wait, it can do something else
- Burst mode allows SDRAM to set up stream of data and fire it out in block
- DDR-SDRAM sends data twice per clock cycle (leading & trailing edge)

IBM 64Mb SDRAM



SDRAM Operation

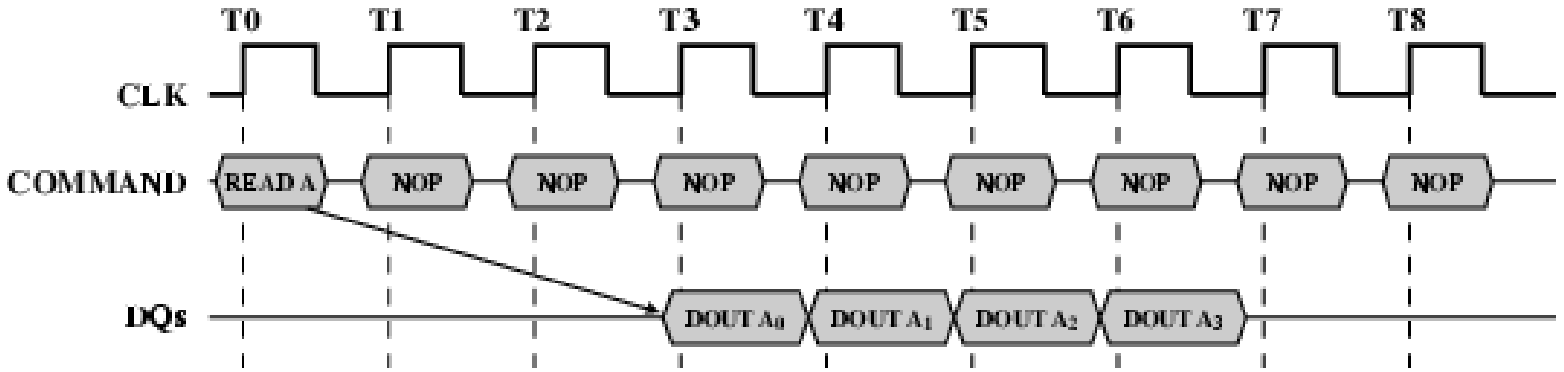


Figure 5.13 SDRAM Read Timing (Burst Length = 4, $\overline{\text{CAS}}$ latency = 2)

RAMBUS

- Adopted by Intel for Pentium & Itanium
- Main competitor to SDRAM
- Vertical package – all pins on one side
- Data exchange over 28 wires < 12 cm long
- Bus addresses up to 320 RDRAM chips at 1.6Gbps
- Asynchronous block protocol
  - 480ns access time
  - Then 1.6 Gbps

RAMBUS Diagram