

EEE 3132 – ASSIGNMENT 01

1. An SRAM has an external organisation of 64K x 1. Draw a diagram showing the internal organisation of the memory. Specifically show the size of the row select, column select, and memory array. Assume that the lower address bits are associated with the row select circuitry. What is the segment size? How many bits make up a physical word? How many bits make up a logical word?
2. The 2114A SRAM is externally organised as a 1024-byte x 4 memory with common I/O. It has only two control inputs, \overline{CS} and \overline{WE} . To read the device, $\overline{CS} = 0$ and $\overline{WE} = 1$. To write the device, $\overline{CS} = 0$ and $\overline{WE} = 0$. Design a 2K x 8 memory system using the 2114A. This memory system should respond only to addresses 0400H to 0BFFH, and its input from the microprocessor are address line A0-A15, bidirectional data lines D0-D7, and control lines \overline{WR} , \overline{RD} , and IO/\overline{M} . Draw a logic diagram of the memory system and label all connections. For address decoding use a 74ALS138 or similar type of decoder. Implement all other logic with standard gates.