RANDOM ACCESS SEMICONDUCTOR MEMORIES

MODULE OUTLINE

1. BASIC MEMORY CONCEPTS
2. STATIC READ WRITE MEMORY, SRAM
3. DYNAMIC RANDOM ACCESS MEMORY, DRAM
4. ADVANCED MEMORY TECHNOLOGIES
5. ERASABLE PROGRAMMABLE READ-ONLY MEMORY, EPROM
6. MEMORY SYSTEM DESIGN
7. MEMORY CLASSES

2.1. BASIC MEMORY CONCCEPTS

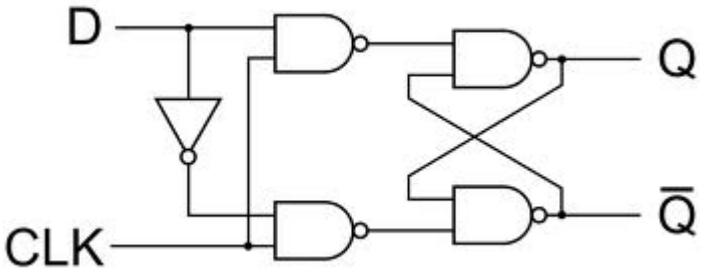
2.1.1. FLIP-FLOP / 1-BIT REGISTER

- **Smallest unit of information is a bit (0 or 1)**
- **Can be stored in a Flip-Flop (ON or OFF)**
- **Common: D-type Flip-Flop, a bistable sub-system or device**

2.1. BASIC MEMORY CONCCEPTS

2.1.1. FLIP-FLOP / 1-BIT REGISTER - contnd

- **Positive clock pulse (0 to 1):**
  - **Leading or Rising edge**
  - **Positive transition**
- **Negative clock pulse (1 to 0):**
  - **Trailing or Falling edge**
  - **Negative transition**



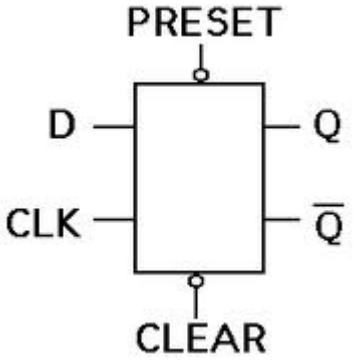


Figure 1: D-type Flip-Flop: (a) Logical diagram; (b) IC Cicuitry

2.1. BASIC MEMORY CONCCEPTS

2.1.1. FLIP-FLOP / 1-BIT REGISTER - contnd

- **Level triggered Flip-Flop: LATCH**
  - **When clock is 1 – Flip-Flop changes its state**
  - **When clock transitions (1 to 0)**
  - **The data present at D input is latched (transferred)**

Figure 1: D-type Flip-Flop: (a) Logical diagram; (b) IC Cicuitry

2.1. BASIC MEMORY CONCCEPTS

2.1.2. m-BIT REGISTERS

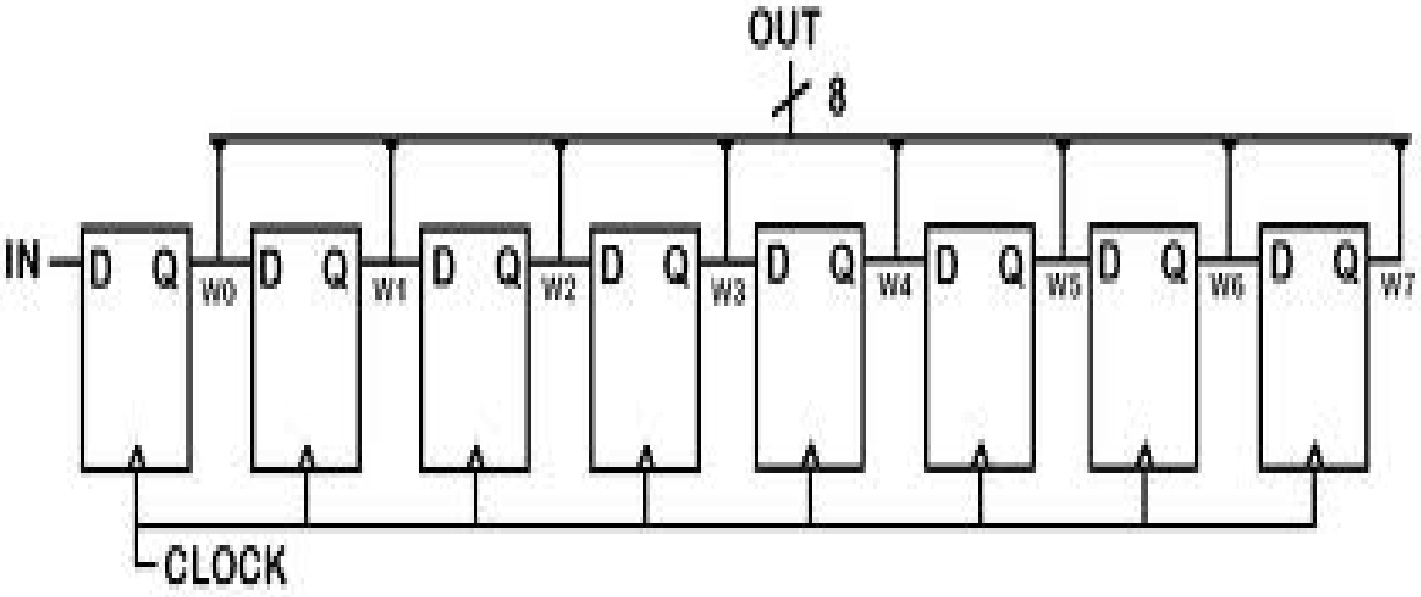


Figure 2: 8-bit (Octal) Register

2.1. BASIC MEMORY CONCCEPTS

2.1.2. m-BIT REGISTERS - contd

- **The m bits make a Word**
- **m is known as a Word length**
- **In digital systems, the Word length is 8 bits = Byte**
- **Half of a byte is known as Nibble**
- **Three-state buffers are buffers (registers) with three output states (0, 1 and undetermined)**

2.1. BASIC MEMORY CONCCEPTS

2.1.3. DATA TRANSFERS BETWEEN REGISTERS

- **Source registers on one side**
- **Destination registers on the other**
- **Data bus between registers – UNIDIRECTIONAL (?)**
- **Data contention (may lead to data corruption)**
- **Common Input to Output registers = DIRECTIONAL Data bus**
- **The memory capacity is measured in bits, byte and its multiple (kB, MB, GB, …)**

2.2. STATIC READ WRITE MEMEORY, SRAM

2.2.1. EXTERNAL ORGANISATION

- **Typical SRAM are of 1, 4 or 8 bits Word Lengths**
- **Pins on a RWM: Address, Data, Control, Power, GND and Clock.**
- **Common I/O often used**

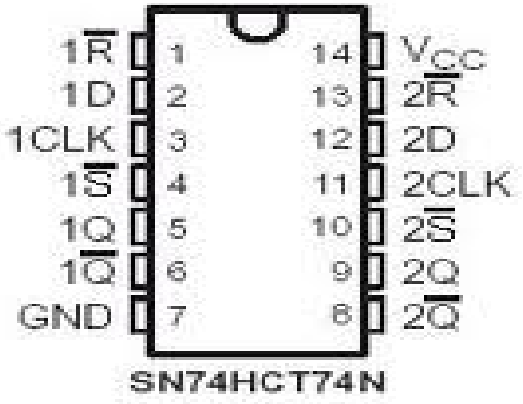


Figure 3: Memory chip

2.2. STATIC READ WRITE MEMEORY, SRAM

2.2.2. INTERNAL ORGANISATION

- **Array of memory cells (1 bit)**
- **Logic to address any memory location.**
- **Circuitry to read content of any address**
- **Circuitry to write to any memory address**
- **Logic circuitries make up logical Word**
- **Physical Word – number of bits**

2.2. STATIC READ WRITE MEMEORY, SRAM

2.2.3. TIMING REQUIREMENTS

A. STEPS FOR MEMORY READ

- Address applied to input.
- SRAM is selected by CS input
- Selected content appears at the output => Access time
- Logic circuitries make up logical Word
- Physical Word – number of bits

2.2. STATIC READ WRITE MEMEORY, SRAM

2.2.3. TIMING REQUIREMENTS

B. STEPS FOR MEMORY WRITE

- **Address applied to input.**
- **SRAM is enabled by logic level of CS input**
- **Input takes data to be written**
- **Write Enable (WE) goes low**
- **Address and CS signals are reallocated**

2.6. COMPUTATION OF TIMING REQUIREMENTS FOR MEMORY

- **READ OPERATION**

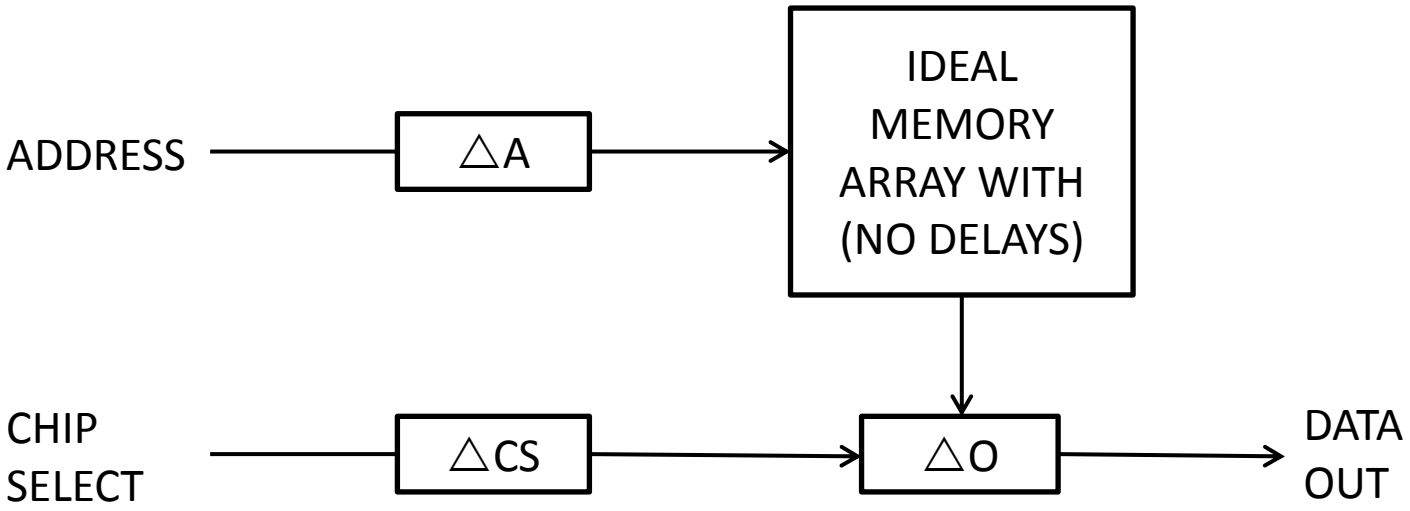


Figure 2.6.1: Lumped delay memory model for a read operation

2.6. COMPUTATION OF TIMING REQUIREMENTS FOR MEMORY

- **READ OPERATION – contd**
  - **Figure 2.6.1 depicts a model of an ideal SRAM (with no delays in signal propagation for a read operation).**
  - **In a real device, there are delays:**
    - **Two input delays: △A and △CS**
    - **One output delay: △O**
  - **Total delay from address application to output is △A + △O**
  - **Total delay from chip select signal to output is △CS + △O**
  - **Let's see timing constraints in the hand-drawn diagram.**

2.6. COMPUTATION OF TIMING REQUIREMENTS FOR MEMORY

- **READ OPERATION – contd**
  - **t_A: Access Time, it's the time elapsed from the subsequent application of an address at the Address Inputs to the appearance at the memory's output of a stable copy of the Address data.**
  - **t_{CO} : Chip Select to Output (Data) valid.**
  - **t_{DF}: Chip Deselect to output Float transition)Time**
  - **t_{OH}: Output Hold from Address change, it's maximum period of previous output data is valid after the address is changed.**
  - **t_{RC}: Read Cycle Time, it specifies the maximum rate at which at which different memory locations can be successfully read.**

2.6. COMPUTATION OF TIMING REQUIREMENTS FOR MEMORY

- **WRITE OPERATION**

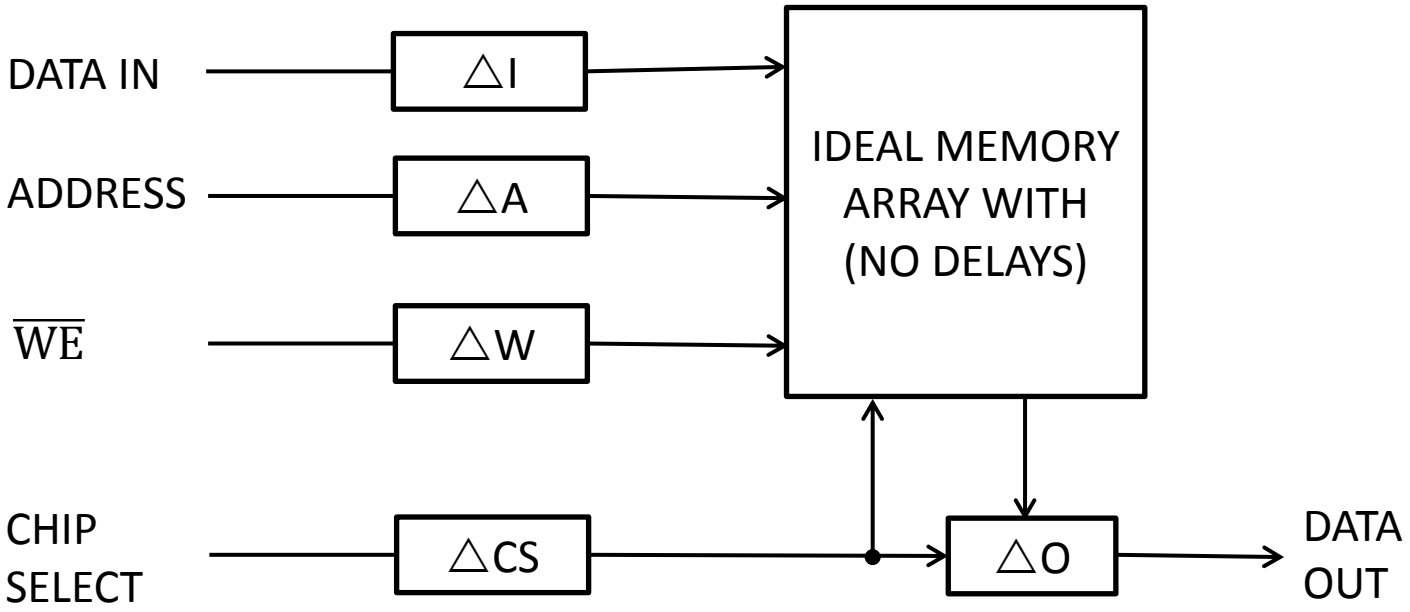


Figure 2.6.2: Lumped delay memory model for a write operation

2.6. COMPUTATION OF TIMING REQUIREMENTS FOR MEMORY

- **WRITE OPERATION – contd**
  - **Figure 2.6.2 depicts a model of an ideal SRAM (with no delays in signal propagation for a write operation).**
  - **In a real device, there are delays:**
    - **Four input delays: △I, △A, △W and △CS**
    - **One output delay: △O**
  - **Number of considerations are in play for a successful write operation**
  - **Delay in changes in input data at the package input pins is given by △I.**
  - **Data stable at the package input pins at least △I - △W earlier.**
  - **For more details on timing constraints, let's see the following hand-drawn digram…**

2.6. COMPUTATION OF TIMING REQUIREMENTS FOR MEMORY

- **READ OPERATION – contd**
  - **t_{AW}: Write delay, indicates how long the address must be stable before the write pulse changes from 1 to 0.**
  - **t_{CW} : Chip Enable to Write Time, indicates how Chip Select stable period before $\overline{WE}$ line changes from 0 to 1.**
  - **t_{DH}: Data Hold from write time, it's the period during the input data is held stable after the $\overline{WE}$ line changes from 0 to 1.**
  - **t_{DW}: Data to Write Time overlap, it's data setup time; this is the period during which data is stabe.**
  - **t_{WCY}: Write Cycle Time, it specifies the minimum time between write operations.**
  - **t_{WP}: Write Pulse Time, it's minimum length of time to guarantee writing into the slowest memory devices.**
  - **t_{WR}: Period during which the address must be held stable after the 0 to 1 transition of $\overline{WE}$.**

2.7. ERASABLE PROGRAMMABLE READ-ONLY MEMORY, EPROM

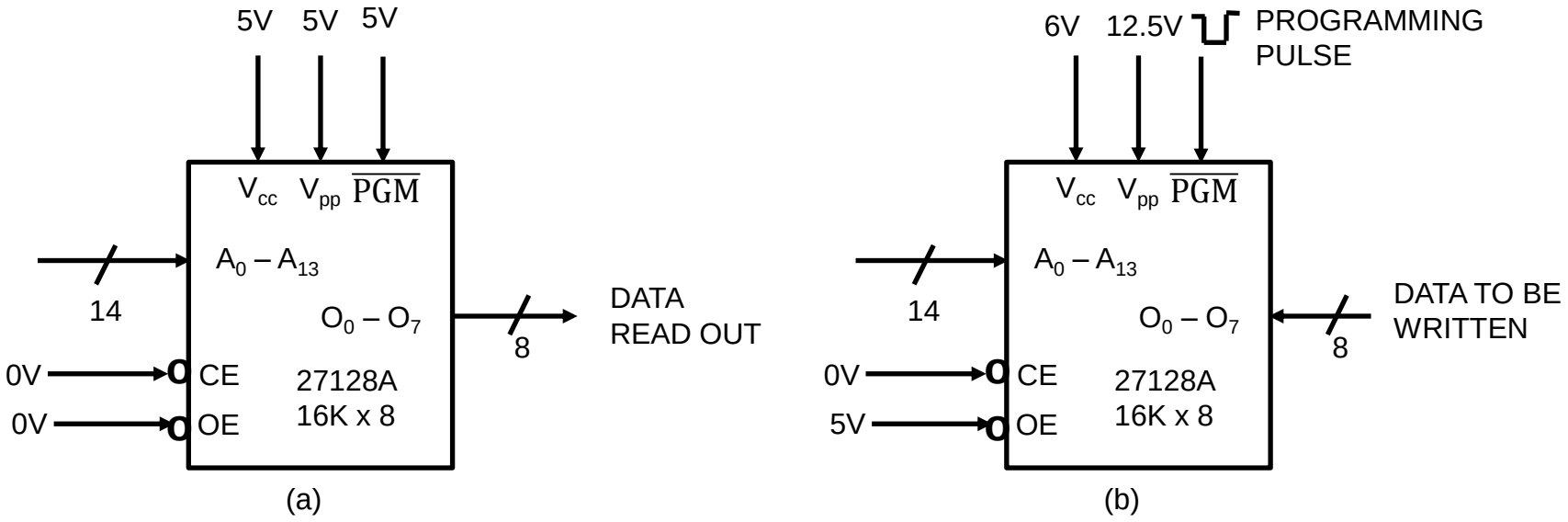
2.7.1. INTRODUCTION

- **EPROM is made by use of ultraviolet light.**
- **EPROM is non-volatile.**
- **Erasure is done by shining ultraviolet light**
- **Must remove EPROM from the microprocessor system before writing o it.**
- **EPROM programmer is special instrument for programming EPPROM chips.**

2.7. ERASABLE PROGRAMMABLE READ-ONLY MEMORY, EPROM

2.7.2. ORGANISATION AND IN-CIRCUIT OPERATION - EPROM's external organisation is similar to SRAM, except there is no $\overline{WE}$.

Figure 27.2.1: 27128A EPROM External connections: (a) Configuration for in-circuit read operation; (b) Configuration for programming on an EPROM programmer



2.7. ERASABLE PROGRAMMABLE READ-ONLY MEMORY, EPROM

2.7.3. EPROM PROGRAMMERS AND INTELLIGENT PROGRAMMERS

- **Generic device programmers.**
- **Two types by their operation mode:**
  - **Standalone programmer**
  - **PC-driven programmer**
- **Microprocessor are critical in programming EPROM.**
- **Intelligent programmers use intelligent algorithms with short pulses.**

2.8. MEMEORY SYSTEM DESIGN

1. Estimate RAM and ROM required
2. Determine address boundaries
3. Select memory devices
4. Determine layout to achieve Word lengths
5. Draw detailed memory mapping
6. Determine buffering requirement
7. Determine memory access speed

2.8. PRACTICAL MEMORY DESIGN

2.8.1. TYPES OF MEMORY DECODING

– Exhaustive Decoding:

- **All address bits are decoded for selection of a memory location**
- **Leads to one-to-one mapping of addresses and memory locations**
- **Also referred to as *fully decoded* memory.**

– Partial Decoding:

- **Not all addresses bits are decoded**
- **Results in simplified decoding logic**
- **Leads to many-to-one mapping of addresses to memory locations.**