the $\overline{OE}$ input. This input is analogous to the output control, $\overline{OC}$, input of the octal registers. Note that the $\overline{WE}$ and $\overline{OE}$ inputs must never be active at the same time.

With the second scheme there is no $\overline{OE}$ input. Whenever the device is selected, $\overline{CS}$ low, it will be written or read, depending on the state of the $\overline{WE}$ input. If $\overline{WE}$ is low, and the device is selected, it is written. Writing of the device usually occurs on the rising edge of either $\overline{WE}$ or $\overline{CS}$, whichever occurs first. If $\overline{WE}$ is high and the device is selected, it is read. The primary advantage of this scheme is to reduce, by one, the number of pins on the device required for control. The advantage of the first scheme is the simplified interconnection of several devices.

2.2.2 Internal Organization

An understanding of the internal organization of semiconductor memory devices leads to a clearer understanding of their operation and timing requirements. SRAMs are designed so that a single device meets all the functional requirements of a memory system. To do so, a device contains

1. An array of memory cells each of which can store a single bit
2. Logic to address any location in the memory
3. Circuitry to allow reading the contents of any memory location
4. Circuitry to allow any memory location to be written

For easy interconnection of a memory device with other memory devices or logic circuits, memory devices contain input drivers, output buffers, and circuitry for address expansion.

SRAMs are internally organized to obtain a memory with high speed, a large bit capacity, and low peripheral circuit and memory array costs [3]. Conceptually, the simplest organization is a ***word organized*** array with ***linear selection***. The memory array in such an organization has a column length equal to the number of

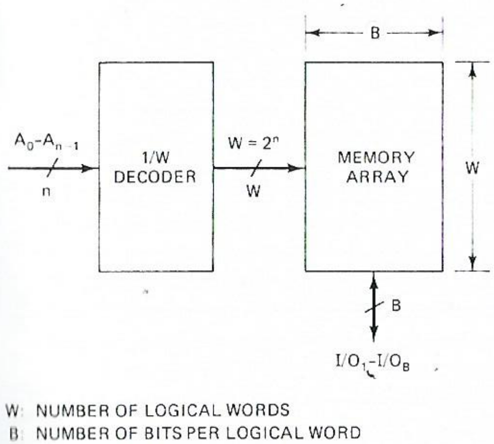

Figure 2.2-2 Internal organization of an SRAM using linear selection. Control logic is not shown.

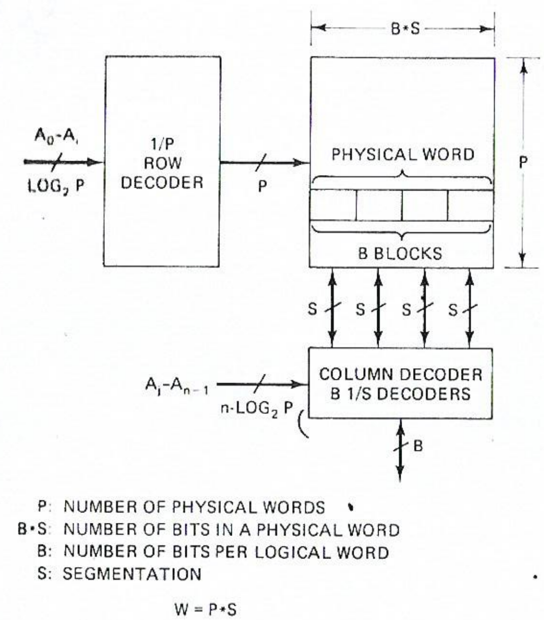

Figure 2.2-3 Two level decoding.

words, W, and a row length equal to the number of bits per word, B (see Fig. 2.2-2). Word selection requires a 1-out-of-W decoder; i.e., a decoder with a mutually exclusive output for each word in the memory. The address inputs to the decoder select one, and only one, of the decoder's outputs—thus selecting one word in the memory array. Clearly, although conceptually simple, the linear selection method requires a large decoder for a large number of words, which is very costly in chip area. For memories with a small number of words, this organization is acceptable and has the advantage of a short access time.

Address decoder size is substantially reduced by organizing the memory array and the word selection logic to allow ***coincident selection*** or ***two-level decoding***. In a memory array utilizing two-level decoding, one level corresponds to a physical word and one to a logical word. A ***physical word*** consists of the number of bits in a row of the memory array. A ***logical word*** consists of the number of bits of a physical word that are sensed and gated to the output at one time. Two-level decoding requires two decoders: a row decoder that selects a physical word and a column decoder, actually several multiplexers, that then selects one logical word from the selected physical word. A physical word is divided into S segments (logical words); the row decoder is a 1-out-of-P decoder, where P is equal to W/S; and the column decoder consists of B, 1-out-of-S multiplexers (see Fig. 2.2-3).

The block diagram of an HM6116 SRAM with 2048, 8-bit words (2 K × 8) organized with two-level decoding is shown in Fig. 2.2-4a [4]. The memory array is 128 × 128 bits; thus, it contains 128 physical words. A physical word is selected by decoding the seven address bits A_1 through A_7. Thus, the row decoder is a