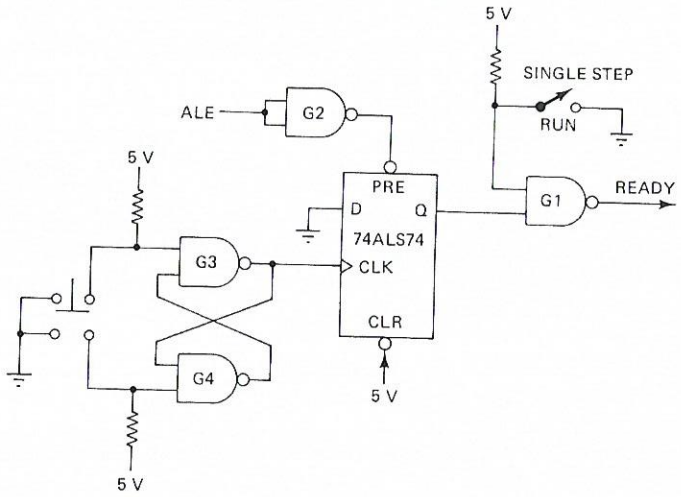

Figure 3.4-7 Hardware single step circuit for the 8085A.

state T_W. It will continue making transitions from T_W back to T_W, staying in the WAIT state until PB1 is pressed again.

The example in Fig. 3.4-8 will be used to illustrate the use of single stepping for hardware troubleshooting and as a further example of instruction execution and machine cycles. Figure 3.4-8 consists of an input device (eight switches), an input port, and address decoding logic. The input port is a 74ALS541 octal buffer. The three-state outputs of the octal buffer are enabled when its enable inputs G1 and G2 are both logic 0. The input device consists of eight single pole switches. Address decoding is implemented using a 74ALS138 1-out-of-8 decoder and a 74ALS30 NAND gate.

A simple ***diagnostic program*** that can be used to test the input port and its associated address decoding logic is shown below:

```
LOOP:   IN SWITCH
        JMP LOOP
```

This is the assembly language representation of the program. LOOP is the address of the first instruction in the program. The program consists of two instructions. The first instruction, IN PORT, inputs data from the switches. SWITCH is the symbol that represents the port address. The port has an 8-bit address, which is F9H. The second instruction, JMP LOOP, causes the microprocessor to jump back and execute the first instruction again. Thus, the program is an infinite loop that executes the two instructions over and over. Assuming the program begins at

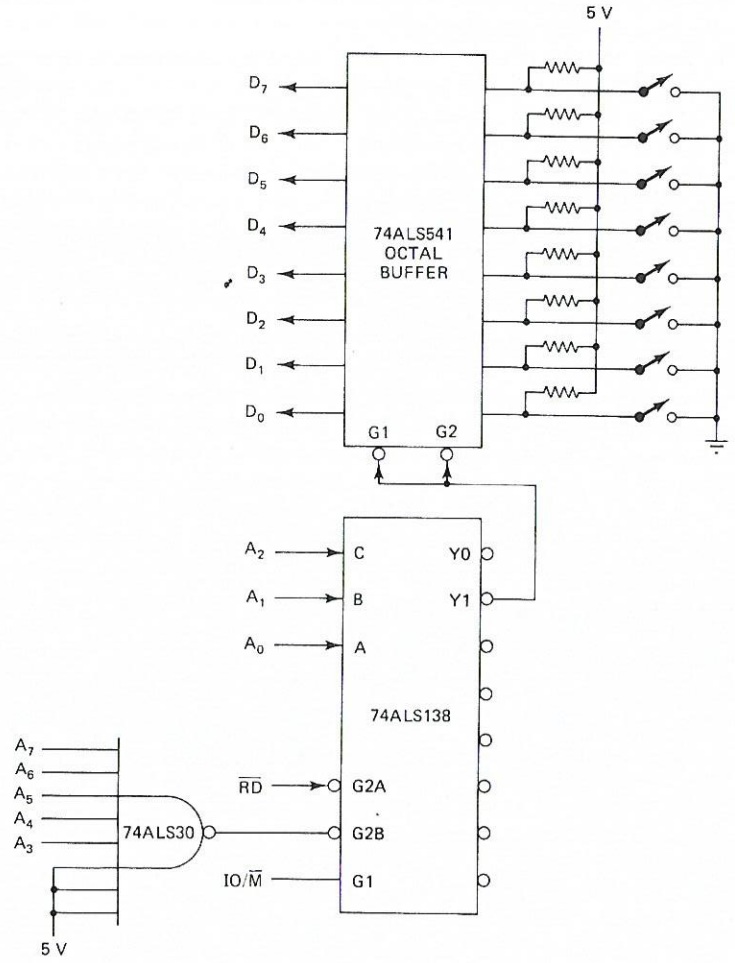

Figure 3.4-8 Input port and associated address decoding logic.

address 0000H, an equivalent representation is

```
IN F9H
JMP 0000H
```

Figure 3.4-9a is a hexadecimal representation of the program code as it appears in memory. The IN instruction is a 2-byte instruction and occupies locations 0000H and 0001H. The first byte, DB, is the opcode for the IN instruction. The second byte, F9H, is the port address. The JMP instruction is a 3-byte