will be used to demonstrate how memory speed requirements can be determined. The memory devices are a 2764A EPROM and a HM6116 SRAM. The objective is to determine the required speeds of these two devices so that no WAIT states are necessary.

The times available for the timing parameters of each memory device must be determined. These times are a function of the timing requirements of the microprocessor and time delays of logic devices that interface the microprocessor to the memory. For each relevant timing parameter of a memory device, a timing equation can be written that relates the memory device's timing parameter to one or more parameters of the microprocessor and time delays of the external logic. For simplicity, the equations are initially written with the time allowed by the microprocessor on the left and the external hardware times on the right. These equations are solved for the memory device's timing parameters. When the times available for each of a memory device's parameters have been found, the slowest memory device that meets these time requirements can be selected.

The times available for the 2764A EPROM will be analyzed first. The timing waveforms and parameter definitions for the 8085AH and 2764A are given in the AC specifications on their data sheets in Appendix F. The 2764A parameter, t_{ACC}, specifies its address to data output delay. From the logic diagram, it can be seen that the address inputs of the 2764A, A_8–A_{12}, are directly driven by the address bits A_8–A_{12} of the microprocessor. However, address inputs A_0–A_7 of the 2764A are driven by address bits A_0–A_7 of the microprocessor, which are delayed by the 74ALS573. Thus, there are two signal paths from the microprocessor to the address inputs of the 2764A. The data outputs of the 2764A are connected directly to the AD_0–AD_7 pins of the microprocessor. The delay allowed from the 8085AH's generation of an address, for a read operation, until valid data must be available at its AD_0–AD_7 pins, is given by the parameter t_{AD}. Thus, the total delay in the external signal path from the 8085AH's address pins back to its data pins must be less than t_{AD} nS. An equation is written for each signal path from the 8085AH's address pins to its data pins and the limiting case determined. The two equations are

$$t_{AD} > t_{ACC} \quad \text{for address bits } A_8\text{–}A_{12}$$

$$t_{AD} > t_{pdL} + t_{ACC} \quad \text{for address bits } A_0\text{–}A_7$$

where t_{pdL} is the worst case propagation delay of the 74ALS573 latch, 14 nS. Solving each of these equations for t_{ACC} gives

$$t_{ACC} < t_{AD}$$

$$t_{ACC} < t_{AD} - t_{pdL}$$

The second equation is the limiting case. Replacing t_{AD} by its equation and solving with $N = 0$ and $T = 325.5$ nS give

$$\begin{aligned} t_{ACC} &< [(5/2 + N) \times T - 225] - 14 \\ &< 574 \text{ nS} \end{aligned}$$

Thus, the access time for the 2764A selected must be less than 574 nS for operation with zero WAIT states.

The parameter t_{CE} for the 2764A specifies the delay from chip enable, $\overline{CE}$, going low until the 2764A provides valid data on the data bus. The signal driving $\overline{CE}$ in the diagram is derived from the A_{13}–A_{15} and IO/$\overline{M}$ outputs of the 8085AH by the 74ALS138. The related 8085AH parameter is again t_{AD}. The equation is

$$t_{AD} > t_{pdD} + t_{CE}$$

where t_{pdD} is the worst case propagation delay of the 74ALS138, 18 nS.

Solving for t_{CE}

$$\begin{aligned} t_{CE} &< t_{AD} - t_{pdD} \\ &< [(5/2 + N) \times T - 225] - 18 \\ &< 570 \text{ nS} \end{aligned}$$

Therefore, t_{CE} for the 2764A selected must be less than 570 nS for zero WAIT state operation.

The 2764A parameter t_{OE} specifies the delay from $\overline{OE}$ going low until its three-state output buffers drive the bus with valid data. Since $\overline{OE}$ is driven directly by $\overline{RD}$ of the 8085AH, and the 8085AH requires valid data within t_{RD} nS after $\overline{RD}$ goes low, the relationship for t_{OE} is simply

$$\begin{aligned} t_{OE} &< t_{RD} \\ &< (3/2 + N) \times T - 180 \\ &< 308.25 \text{ nS} \end{aligned}$$

The delay from either $\overline{CE}$ or $\overline{OE}$ going high until the 2764A's three-state output buffers are disabled is t_{DF}. Since $\overline{OE}$ will go high before $\overline{CE}$ in this system, the related 8085AH parameter is the time from $\overline{RD}$ going high until some device other than the 2764A subsequently drives the data bus. Examination of the 8085AH read timing diagram indicates that the data bus will next be driven by the microprocessor with the address bits A_0–A_7 for the next machine cycle. This time is specified by the parameter t_{RAE}. Thus

$$t_{RAE} > t_{DF}$$

Solving for t_{DF}

$$\begin{aligned} t_{DF} &< t_{RAE} \\ &< (1/2) \times T - 10 \\ &< 152.75 \text{ nS} \end{aligned}$$

If the 2764A selected requires more than 152.75 nS to disable its output buffers, bus contention would result between the 8085AH and the 2764A.

The parameter t_{OH} indicates how long the 2764A will continue to provide valid output data after $\overline{RD}$ goes high. This parameter must be compared to the data