types of memory just discussed. Each of those memory types is noted for certain advantages in terms of economics and performance in particular applications.

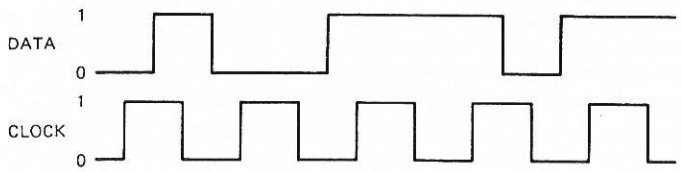
REFERENCES

1. W. I. Fletcher, *An Engineering Approach to Digital Design* (Englewood Cliffs, N.J.: Prentice-Hall, 1980).
2. *The TTL Data Book*, Vol. 3 (Dallas, Tex.: Texas Instruments, Inc., 1984).
3. R. E. Matick, "Memory and Storage," in *Introduction to Computer Architecture*, ed. H. S. Stone (Chicago: Science Research Associates, Inc., 1975), chap. 5.
4. *IC Memories Data Book* (San Jose, Calif.: Hitachi America, Ltd).
5. *Memory Components Handbook* (Santa Clara, Calif.: Intel Corporation, 1985).
6. P. Alfke and I. Larsen, eds., *The T^2L Applications Handbook* (Mountain View, Calif.: Fairchild Semiconductor, 1973).
7. D. Frohman-Bentchkowsky, "A Fully Decoded 2048-Bit Electrically Programmable FAMOS Read-Only Memory," *IEEE Journal of Solid State Circuits*, SC-6, (October 1971), 301–06.
8. M. H. Woods, "An E-PROM's Integrity Starts with Its Cell Structure," *Electronics*, August 14, 1980.

PROBLEMS

2-1. Draw a block diagram showing the common bus structure of a microprocessor based system and the subsystems that the bus connects. Each of the subsystems consists of registers. For each subsystem indicate the nature of the registers that make up the system, i.e., read only, write only, read write, storage, operational, and so on.

2-2. For the clock and data waveforms below draw the output waveform, Q, for a D-type flip-flop for each of the following types of triggering:
(a) positive edge triggered
(b) negative edge triggered
(c) positive level triggered
Assume $Q = 0$ initially.



2-3. Draw a logic diagram showing the connection of four 74ALS574 positive edge triggered octal D-type flip-flops, so that the resulting circuit has separate I/O. The input bus is driven by SPST switches and the output bus drives indicator lights. Design logic that will allow any of the registers to be written by a write strobe, $\overline{WR}$, and will allow any register to drive the indicator lights during a read strobe, $\overline{RD}$. Writing and reading of the registers can occur simultaneously. The register written and the register read need not be the same. Use a 74ALS139 dual 1-out-of-4 decoder and any other necessary SSI gates to implement any required logic.

2-4. Give the number of address bits required to address any word in a memory that contains the following number of words:
(a) 1024
(b) 4096
(c) 512
(d) 8192
(e) 64,536

2-5. List the hexadecimal equivalents of the following memory addresses specified in decimal:
(a) 123
(b) 750
(c) 2048
(d) 6743

2-6. Draw a timing diagram showing the relative timing relationships of the data and clock for a positive edge triggered D-type flip-flop. The clock signal is a negative pulse. Label the diagram to show hold time, minimum write pulse width, and setup time. Show the data in the high impedance state except when data must be valid. Draw a second timing diagram for the write operation of a RWM. This diagram should show address, data, and active low write strobe. Label the diagram to show hold time, minimum write pulse width, setup time, and write cycle time.

2-7. A 256 × 4 memory can be organized using linear selection or two-level decoding.
(a) Draw a block diagram of the logical organization of the memory if linear selection is used.
(b) If two-level decoding is used and the memory array consists of 32 physical words, draw a block diagram of the logical organization of the memory; specify all appropriate parameters and the method of segmentation.

2-8. Draw a block diagram of the internal structure of a 1024 × 1 SRAM that uses a square memory array and two-level decoding. List the size and number of all required decoders and the address inputs associated with each.

2-9. An SRAM has an external organization of 64 K × 1. Draw a diagram showing the internal organization of the memory. Specifically show the size of the row select, column select, and memory array. Assume that the lower address bits are associated with the row select circuitry. How many bits make up a physical word? How many bits make up a logical word?

2-10. An SRAM has an external organization of 1 K × 4. Draw a diagram of the internal organization of the memory. Show the size of the row select, column select, and memory array. Associate the low order address bits with the row select circuitry. Specify the number of logical words and physical words. Specify the number of bits in a logical word and the number of bits in a physical word. What is the segmentation value? How may multiplexers exist in the circuit, and what is their size?