ADDRESS	CODE	COMMENT
0000	DB	IN OPCODE
0001	F9	PORT ADDRESS
0002	C3	JMP OPCODE
0003	00	LOW BYTE OF JUMP ADDRESS
0004	00	HIGH BYTE OF JUMP ADDRESS

(a)

MACHINE CYCLE	ADDRESS BUS	DATA BUS
OPCODE FETCH	0000	DB
MEMORY READ	0001	F9
INPUT	F9F9	XX ← DATA VALUES READ FROM SWITCH
OPCODE FETCH	0002	C3
MEMORY READ	0003	00
MEMORY READ	0004	00
OPCODE FETCH	0000	DB ← LOOP REPEATS

(b)

Figure 3.4-9 (a) Test program. (b) Machine cycle type and address and data bus contents.

instruction and occupies locations 0002H through 0004H. The first byte, C3, is the opcode for a JMP instruction. The second and third bytes are the low and high bytes of the address from which the next instruction will be fetched.

Execution of the 2-byte IN instruction requires three machine cycles. The first two machine cycles, an OPCODE FETCH and a MEMORY READ, fetch the instruction. The third machine cycle, an I/O READ, inputs the data from the port. Figure 3.4-9b lists the machine cycles in their order of occurrence. This figure also shows the values that would appear on the address bus and data bus during the WAIT state when the program is single stepped.

To troubleshoot the hardware, the program can be single stepped until the third machine cycle. At this point, the address bus should have the value F9F9H. This occurs because during the I/O READ machine cycle the 8085A replicates the port address on both the high and low bytes of the address bus. The occurrence of the port address can be verified by checking the bits of the address bus with a logic probe. During an I/O READ machine cycle, IO/M is logic 1, indicating that the address on the address bus is an I/O address instead of a memory address. During the WAIT state, the RD strobe will be held at logic 0.

With the above conditions present, the enable inputs G1 and G2 of the octal buffer should be logic 0. If this is the case, then the logic value of each switch should appear on its corresponding data bus bit. The switch values can be changed and the corresponding changes should occur on the data bus bits. This test provides reasonable confidence that the address decoding logic, octal buffer, and switches are operating properly. If G1 and G2 are not logic 0 and the inputs to the address decoding logic have the correct values, then either the NAND gate or 1-out-of-8 decoder or their associated connections is the problem. A logic probe can be used to trace through the address decoding logic to determine if a connection or IC is bad.

An alternate approach to verifying proper circuit operation can be taken using the same diagnostic program. In this case the program is not single stepped but is executed in the normal manner. With the program continuously running, signals supplied to and generated by the circuit are again traced using the logic probe. However, with this dynamic approach, pulses or strobes are traced through the circuit rather than static logic levels.

3.5 MEMORY SPEED REQUIREMENTS

In Section 2.4 the logic design of memory systems was presented without consideration of the memory speed required for an application. Since the microprocessor controls the system timing, determination of memory speed requirements can only be made in the context of the microprocessor system in which the memory is used. Figure 3.5-1 shows the memory system of Fig. 2.4-2 interfaced to an 8085AH, and

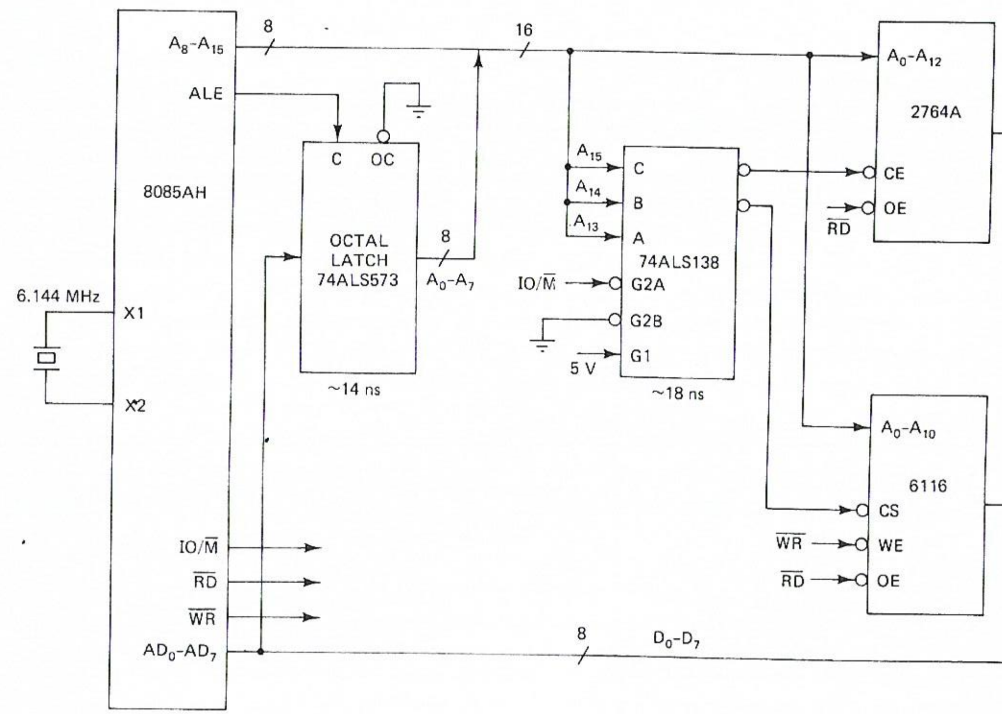

Figure 3.5-1 Memory system interfaced to an 8085AH.