EEE 3131 DIGITAL ELECTRONICS

SOLUTIONS TO TERM 1 TEST – 2014/2015 ACADEMIC YEAR - DECEMBER, 2014

QUESTION 1

a)

(i) Convert the decimal number 429.3125_{10} to its binary equivalent. **[5 Marks]**

(ii) Hence, determine the hexadecimal equivalent of the decimal number in (i) above. **[5 Marks]**

(iii) Find the octal equivalent of the decimal number 153.9795_{10}, correct to four (4) octal point places. **[5 Marks]**

SOLUTION:

(i) The decimal number 429.3125_{10} is converted to its binary equivalent by converting whole and fractional numbers as shown below:

2	429	remainder
	214	1
	107	0
	53	1
	26	1
	13	0
	6	1
	3	0
	1	1
	0	1

	Product	Carry
2×0.3125	0.625	0
2×0.625	1.25	1
2×0.25	0.5	0
2×0.5	1.0	1

Therefore, $429.3125_{10} = \mathbf{110101101.0101_2}$ **[5 Marks]**

(ii) Thus, the hexadecimal equivalent of 429.3125_{10} is obtained as follows:

0001 1010 1101. 0101

1 A D . 5

Therefore, $429.3125_{10} = \mathbf{1AD.5}$ in hexadecimal. **[5 Marks]**

(iii) The octal equivalent of the decimal number 153.9795_{10} is obtained by converting the whole and fractional parts as indicated below.

8	153	remainder
	19	1
	2	3
	0	2

	Product	Carry
8×0.9795	7.8360	7
8×0.8360	6.6880	6
8×0.6880	5.504	5
8×0.504	4.032	4
8×0.032	0.256	0

Therefore, $153.9795_{10} = \mathbf{231.7654}$ in octal form correct to 4 octal points. **[5 Marks]**

b) Simplify the following three variable Boolean expressions using the Karnaugh map method and draw their respective simplified logic circuits

(i) $F = A\overline{B} + \overline{A}\,\overline{B} + AB\overline{C} + \overline{A}BC$ **[5 Marks]**

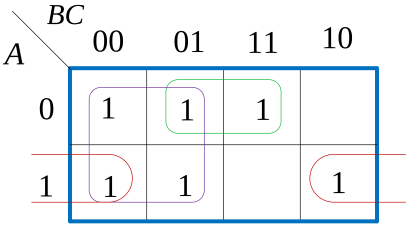
(ii) $F = \overline{A}C + B\overline{C} + \overline{A}B$ **[5 Marks]**

SOLUTION:

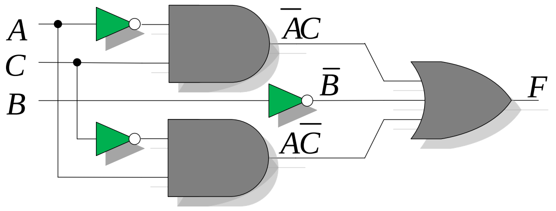
(i) First of all we express $F = A\overline{B} + \overline{A}\,\overline{B} + AB\overline{C} + \overline{A}BC$ in canonical form before simplifying it using the K-map. That is,

$F = A\overline{B}\left(C + \overline{C}\right) + \overline{A}\,\overline{B}\left(C + \overline{C}\right) + AB\overline{C} + \overline{A}BC$, implying that,

$F = A\overline{B}C + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}C + \overline{A}\,\overline{B}\,\overline{C} + AB\overline{C} + \overline{A}BC$. It follows that the Karnaugh map is of the form,



A \ BC	00	01	11	10
0	1	1	1	
1	1	1		1



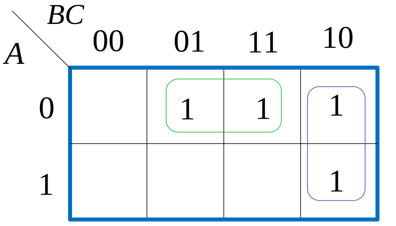
Therefore, the simplified expression is, $F = \overline{B} + \overline{A}C + A\overline{C}$, the circuit implementation of which is as shown above.

[5 Marks]

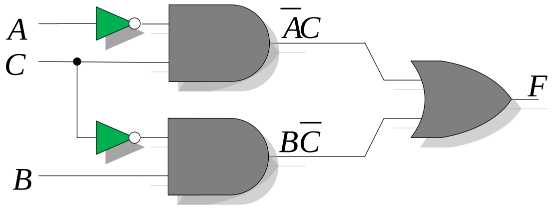
(ii) Expressed in canonical form, $F = \overline{A}C + B\overline{C} + \overline{A}B$ is as shown:

$F = \overline{A}C\left(B + \overline{B}\right) + B\overline{C}\left(A + \overline{A}\right) + \overline{A}B\left(C + \overline{C}\right)$, that is to say,

$F = \overline{A}BC + \overline{A}\,\overline{B}C + AB\overline{C} + \overline{A}B\overline{C} + \overline{A}BC + \overline{A}B\overline{C}$. It follows that the Karnaugh map is of the form,



A \ BC	00	01	11	10
0		1	1	1
1				1



Therefore, the simplified expression is $F = \overline{A}C + B\overline{C}$, the circuit implementation of which is as shown above.

[5 Marks]

[Total 25 Marks]

QUESTION 2

a) Subtraction in binary can be performed by addition of signed 2's complement of operands.

(i) Using signed 2's complement notation, express as 8 bit words the decimal numbers 33 and -161. **[5 Marks]**

(ii) Hence, perform in 2's complement notation the arithmetic operation $33 - 161$. **[5 Marks]**

SOLUTION:

(i) The 8 bit 2’s complement notation of 33 and -161 are obtained as follows,

2	33	remainder
	16	1
	8	0
	4	0
	2	0
	1	0
	0	1

2	161	remainder
	80	1
	40	0
	20	0
	10	0
	5	0
	2	1
	1	0
	0	1

Therefore, $33 = \mathbf{00100001}$ in 8 bit 2’s complement notation. **[2.5 Marks]**

Similarly, $161_{10} = 10100001_2$, whose 1’s complement is 01011110. Finally, the 2’s complement is $01011110 + 1 = 01011111$.

Therefore, $-161_{10} = \mathbf{01011111_2}$ in 8 bit 2’s complement notation. **[2.5 Marks]**

(ii) Hence, the 2’s complement arithmetic operation $33-161$ is performed as follows:

$$\begin{array}{r} \text{2's compl} \\ \hline \mathbf{00100001} \\ \mathbf{+\,01011111} \\ \hline \mathbf{10000000} \end{array} \qquad \begin{array}{r} \text{1's compl} \\ \hline \mathbf{10000000} \\ \mathbf{-\qquad 1} \\ \hline \mathbf{01111111} \end{array}$$

Since there is no carry, and the MSB is 1, the answer is presumably negative. Thus, the 1’s complement is found as shown above. Finally, the actual magnitude is obtained by taking the 1’s complement of $\mathbf{01111111}$.
Therefore, the actual magnitude is $-\mathbf{10000000}$ **[5 Marks]**

b) The sum of products Boolean expression in short form notation is given by $f(A,B,C,D,E) = \sum 1,5,16,20 + \sum_d 0,4,17,21$, where the second summation over d denotes the ‘don’t care’ conditions.

(i) Draw the Minterm Karnaugh map for the given expression. **[8 Marks]**

(ii) Using the Karnaugh map in (i) find the minimized Boolean expression. **[4 Marks]**

(iii) Hence, draw the minimized logic circuit. **[3 Marks]**

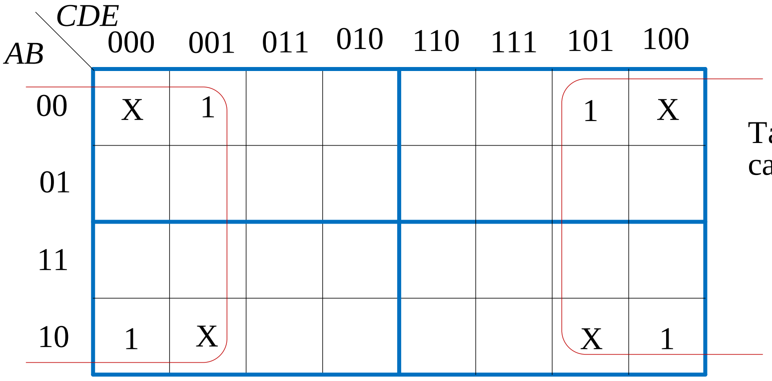
[Total 25 Marks]

SOLUTION:

(i) Given SOP Boolean expression in short form notation as $f(A,B,C,D,E) = \sum 1,5,16,20 + \sum_d 0,4,17,21$, its expanded form is as shown

$$f(A,B,C,D,E) = \sum[00001,\ 00101,\ 10000,\ 10100]$$
$$+\sum_d[00000,\ 00100,\ 10001,\ 10101]$$ **[4 Marks]**

Thus, the Karnaugh map is as shown:



AB \ CDE	000	001	011	010	110	111	101	100
00	X	1					1	X
01								
11								
10	1	X					X	1

Take all don't cares to be 1's

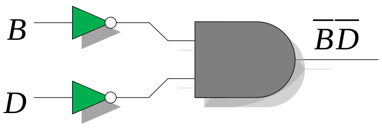
[4 Marks]

(ii) From the Karnaugh map only one group is formed, thus the simplified expression is given by,

$$f\left(A,B,C,D,E\right)=\bar{B}\bar{D}$$

[4 Marks]

(iii) Consequently, the minimized logic circuit is found to be



[3 Marks]

[Total 25 Marks]

QUESTION 3

a) Convert the Binary number 11001111_2 to its Gray code equivalent. **[3 Marks]**

SOLUTION:

(a) The conversion of the binary number 11001111_2 to Gray code is obtained as follows:

Step 1: The MSB of the Gray code is the same as that of the Binary number.
Step 2: The second MSB of the Gray code is obtained from the sum of the MSB and the second MSB of the binary number, ignoring the carry.
Step 3: The other bits of the Gray code in similar fashion to step 2.

Therefore, $11001111_2 = \mathbf{10101000}$ in Gray code. **[3 Marks]**

b) The Boolean expression for a two-input OR gate is given by $F = A + B$, where A and B are input logic variables and F the output.

(i) With the aid of appropriate Boolean laws and theorems modify the given expression so as to implement a two-input OR gate using two-input NAND gates only.

[4 Marks]

(ii) Hence, draw the logic circuit implementation of a two-input OR gate using two-input NAND gates only. **[4 Marks]**

SOLUTION:

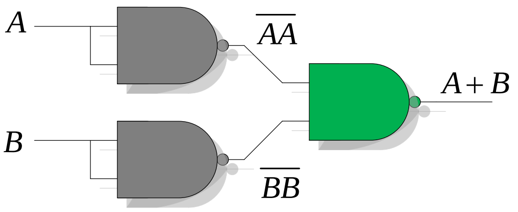
(b) Given the two-input OR gate expression $Y = A + B$

i) $Y = A + B = \overline{\overline{A}} + \overline{\overline{B}}$, by the Involution law, It follows that $\overline{\overline{A}}+\overline{\overline{B}}=\overline{\overline{A}\cdot\overline{B}}$, by DeMorgan's theorem,

By the Idempotent law, $\overline{\overline{A}}\cdot\overline{\overline{B}}=\overline{(\overline{A\cdot A})\cdot(\overline{B\cdot B})}$.

Therefore, the modified form given as $Y=\overline{(\overline{A\cdot A})\cdot(\overline{B\cdot B})}$ **[4 Marks]**

ii) Thus, the logic circuit is as shown below.



[4 Marks]

c) Write the 16-bit excess-3 equivalent codes for the following decimal numbers

(i) 4_{10} **[3 Marks]**

(ii) 423_{10} **[3 Marks]**

SOLUTION:

(i) Begin by converting 4_{10} to its 16-bit binary equivalent, i.e.,

$4_{10}=0000\,0000\,0000\,0100$, thus by adding 0011 to each of the 4-bits we obtain:

$$\begin{array}{r} 0000\ \ 0000\ \ 0000\ \ 0100 \\ +\ \ 0011\ \ 0011\ \ 0011\ \ 0011 \\ \hline \mathbf{0011\ \ 0011\ \ 0011\ \ 0111} \end{array}$$

[3 Marks]

(ii) Similarly, $423_{10}=0423_{10}$, adding 3 to each digit yields '3', '7', '5', and '6' which when converted to their binary equivalents gives the Excess-3 code, i.e.,

$423_{10}=$ **0011 0111 0101 0110** in Excess-3 code. **[3 Marks]**

d) Simplify the Boolean expression $F=A\overline{B}C+\overline{A}\overline{B}C+AB\overline{C}+\overline{A}BC+ABC+\overline{A}\overline{B}\overline{C}$ using appropriate Boolean laws and theorems. Hence, draw the simplified logic circuit.

[8 Marks]

[Total 25 Marks]

SOLUTION:

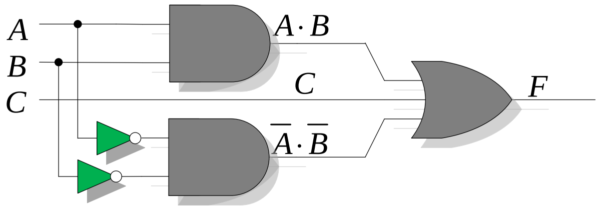
The expression $F=A\overline{B}C+\overline{A}\overline{B}C+AB\overline{C}+\overline{A}BC+ABC+\overline{A}\overline{B}\overline{C}$ is simplified as follows:

By the distributive law, the second and last terms, and the third and fifth terms are combined to yield, $F=A\overline{B}C+\overline{A}\overline{B}\left(C+\overline{C}\right)+AB\left(C+\overline{C}\right)+\overline{A}BC$.

But $\left(C+\overline{C}\right)=1$, thus $F=AB+A\overline{B}C+\overline{A}\overline{B}+\overline{A}BC$. Once again applying the distributive law we obtain, $F=A\left(B+\overline{B}C\right)+\overline{A}\left(\overline{B}+BC\right)$. Furthermore, applying the distributive law yields,

$F = A\left(B+C\right)+\bar{A}\left(\bar{B}+C\right)$. Therefore, $F = AB+\bar{A}\bar{B}+C$ **[4 Marks]**

Thus the circuit implementation is as shown below:



[4 Marks]

[Total 25 Marks]

QUESTION 4

a) Divide $\left(100.0001\right)_2$ by $\left(10.1\right)_2$ using long division method. **[4 Marks]**

SOLUTION:

Before we apply the long division, the binary point in both the divisor and dividend is moved by one step to the right as shown below:

$$\begin{array}{r} 1.101 \\ 101\overline{)1000.001} \\ \underline{101} \\ 110 \\ \underline{101} \\ 101 \\ \underline{101} \\ 0 \end{array}$$

[4 Marks]

b) Given a product of sums (POS) Boolean expression in short form notation as

$f\left(A,B,C,D\right)=\prod 1,3,4,6,9,11,12,14$,

(i) Write the POS Boolean expression in canonical form. **[4 Marks]**

(ii) Draw the product of sums Karnaugh map. **[4 Marks]**

(iii) Hence find the minimized Boolean expression. **[3 Marks]**

SOLUTION:

(i) The POS expression in canonical form given, $f\left(A,B,C,D\right)=\prod 1,3,4,6,9,11,12,14$, is

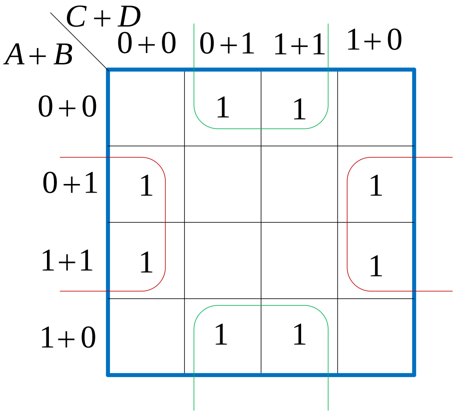
$$f\left(A,B,C,D\right)=\left(0+0+0+1\right)\cdot\left(0+0+1+1\right)\cdot\left(0+1+0+0\right)\cdot\left(0+1+1+0\right)$$
$$\cdot\left(1+0+0+1\right)\cdot\left(1+0+1+1\right)\cdot\left(1+1+0+0\right)\cdot\left(1+1+1+0\right)$$

That is,

$$f\left(A,B,C,D\right)=\left(A+B+C+\bar{D}\right)\cdot\left(A+B+\bar{C}+\bar{D}\right)\cdot\left(A+\bar{B}+C+D\right)\cdot\left(A+\bar{B}+\bar{C}+D\right)$$
$$\cdot\left(\bar{A}+B+C+\bar{D}\right)\cdot\left(\bar{A}+B+\bar{C}+\bar{D}\right)\cdot\left(\bar{A}+\bar{B}+C+D\right)\cdot\left(\bar{A}+\bar{B}+\bar{C}+D\right)$$

[4 Marks]

(ii) The POS Karnaugh map is thus of the form shown below.



$C+D$ $A+B$	$0+0$	$0+1$	$1+1$	$1+0$
$0+0$		1	1	
$0+1$	1			1
$1+1$	1			1
$1+0$		1	1	

[4 Marks]

Product-of-sums K-map

(iii) Therefore, the minimized expression from the above Karnaugh map is of the form,
$f(A,B,C,D)=\left(\overline{B}+D\right)\cdot\left(B+\overline{D}\right)$. **[3 Marks]**

c) A two-input EX-OR gate has the Boolean equation $F=\overline{A}B+A\overline{B}$

(i) Apply suitable Boolean laws and theorems to modify the expression for a two-input EX-OR gate in such a way as to implement a two-input EX-OR gate by using the minimum number of two-input NAND gates only. **[5 Marks]**

(ii) Draw the resultant logic circuit. **[5 Marks]**

SOLUTION:

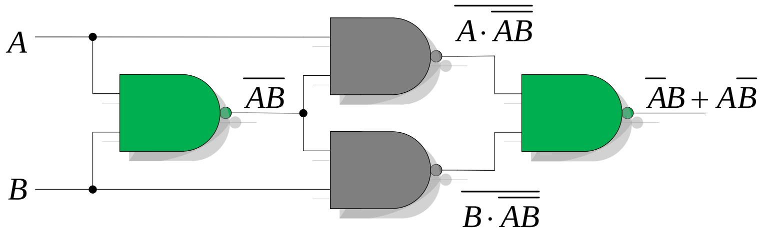
(i) Given the EX-OR expression $F=\overline{A}B+A\overline{B}$, it follows that,

$$F=\overline{A}B+A\overline{B}=\overline{\overline{\overline{A}B}}+\overline{\overline{A\overline{B}}}$$ by the Involution law.

$$F=\overline{\overline{\overline{A}\cdot B}\cdot\overline{A\cdot\overline{B}}}$$, by DeMorgan’s law.

Therefore, $$F=\overline{\overline{\left[B\cdot\left(\overline{A}+\overline{B}\right)\right]}\cdot\overline{\left[A\cdot\left(\overline{A}+\overline{B}\right)\right]}}=\overline{\overline{\left[B\cdot\overline{A\cdot B}\right]}\cdot\overline{\left[A\cdot\overline{A\cdot B}\right]}}$$ **[5 Marks]**

(ii) The circuit implementation is thus as shown below.



[5 Marks]

[Total 25 Marks]

Compliments of the season!