EEE 3132 – DIGITAL ELECTRONICS
MODEL SOLUTIONS TO FINAL EXAMINATION - 2013/2014 ACADEMIC YEAR
DATE OF EXAMINATION: JULY, 2014

QUESTION 1 [SOLUTION]

a)

i) The Excess-3 equivalent codes of 6_{10} and 537_{10} in 16-bit format given by:

- $6_{10} = 0006_{10}$, adding 3 to each digit yields, '3', '3', '3' and '9'.

  Thus the corresponding 4-bit binary equivalents are '0011', '0011', '0011' and '1001.

  Therefore, 6_{10} in 16-bit format Excess-3 code is **0011001100111001** **[2 Marks]**

- $537_{10} = 0537_{10}$, adding 3 to each digit yields, '3', '8', '6' and '10'.

  Thus the corresponding 4-bit binary equivalents are '0011', '1000', '0110' and '1010'.

  Therefore, 537_{10} in 16-bit format Excess-3 code is **0011100001101010** **[2 Marks]**

ii) The decimal number 27.5625 is converted to its binary equivalent by converting whole and fractional numbers as shown below:

2	27	remainder
	13	1
	6	1
	3	0
	1	1
	0	1

	Product	Carry
2×0.5625	1.125	1
2×0.125	0.25	0
2×0.25	0.5	0
2×0.5	1.0	1

Therefore, $27.5625_{10} = \mathbf{11011.1001_2}$ **[3 Marks]**

b) Analysis of the Spacecraft triple sensing system yields :

i) The truth-table for the spacecraft triple sensing system, taking **0** to denote '**no action**' and **1** to denote '**action**' is given as

Truth-table

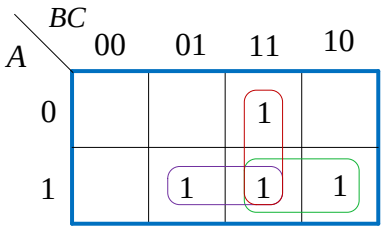
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

[3 Marks]

ii) From the truth table the minterm (sum-of-products) Boolean expression is given by

$$Y = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$$ **[2 Marks]**

iii) Using the Karnaugh map method Boolean expression is simplified as

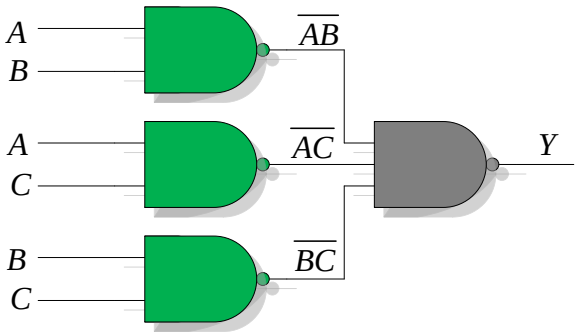


Based on the K-map the simplified expression is $Y = AB + AC + BC$ **[4 Marks]**

iv) By DeMorgan's theorem, $\overline{\overline{AB} \cdot \overline{AC} \cdot \overline{BC}} = \overline{\overline{AB}} + \overline{\overline{AC}} + \overline{\overline{BC}} = AB + AC + BC$, thus,

$$Y = AB + AC + BC = Y = \overline{\overline{AB} \cdot \overline{AC} \cdot \overline{BC}}.$$ **[2 Marks]**

v) Finally the logic circuit for the expression obtained in (iv) is as shown below.



[2 Marks]

[Total 20 Marks]

QUESTION 2 [SOLUTION]

a) Subtraction in 2's complement is achieved as follows:

i) 25 and –87 are converted to signed 2's complement notation, express as 8 bit words, i.e.,

2	25	remainder
	12	1
	6	0
	3	0
	1	1
	0	1

Therefore, the 2's complement of 25 in 8 bit format is **00011001**. **[2 Marks]**

2	87	remainder
	43	1
	21	1
	10	1
	5	0
	2	1
	1	0
	0	1

Thus, $87_{10} = 01010111_2$ in 8 bit format and its 1's complement is 10101000.

It follows that the 2's of -87_{10} is $10101000 + 1 = 10101001$.

Therefore, the 2's complement of -87_{10} in 8 bit format is **10101001**. **[2 Marks]**

ii) It follows that the arithmetic operation $25 - 87$ in 2's complement is as follows:

2's compl
00011001
+ 10101001
11000010

1's compl
11000010
– 1
11000001

[2 Marks]

There is no carry, and MSB is 1, thus the answer is negative. Thus, the 1's complement is shown above.

Finally, the actual magnitude is obtained by taking the 1's complement of **11000001**.

Therefore, the actual magnitude is **-01000110**. **[2 Marks]**

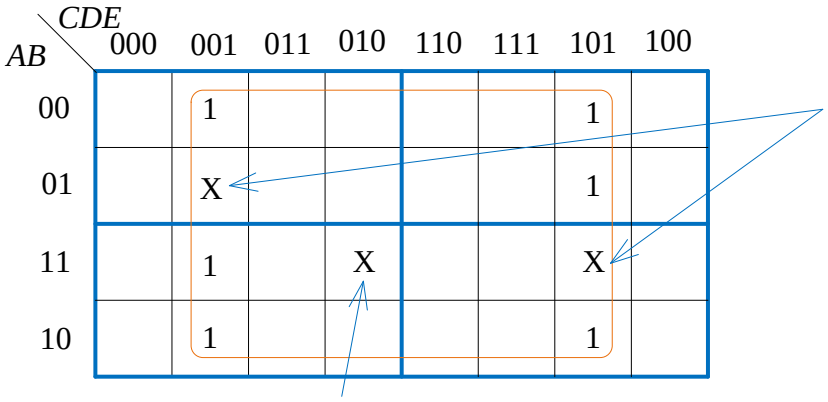
b) Given sum of products Boolean expression in short form notation as

$f(A,B,C,D,E) = \sum 1,5,13,17,21,25 + \sum_d 9,26,29$, where the second summation over d denotes the 'don't care' conditions.

i) The Minterm Karnaugh map is realized from the expanded form of the expression as follows:

$$f(A,B,C,D,E) = \sum[00001,\ 00101,\ 01101,\ 10001,\ 10101,\ 11001] + \sum_d[01001,\ 11010,\ 11101]$$

[3 Marks]



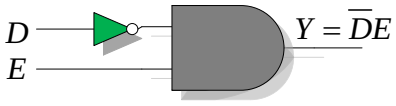
[5 Marks]

ii) From the Karnaugh map in (i) only one group is formed thus the simplified expression is given by,

$$f(A,B,C,D,E) = \overline{D}E$$

[2 Marks]

iii) As a consequence the minimized logic circuit found to be:



[2 Marks]

[Total 20 Marks]

QUESTION 3 [SOLUTION]

a)

i) To determine the octal equivalent of the decimal number 93.75 the whole and fractional numbers are converted as shown below:

8	93	remainder
	11	5
	1	3
	0	1

	Product	Carry
8×0.75	6.0	6

Therefore, $93.75_{10} = \mathbf{135.6_8}$ **[3 Marks]**

ii) The product of binary numbers 1101.01 and 10.1 is

$$\begin{array}{r} 1101.01 \\ \times \quad 10.1 \\ \hline 110101 \\ 000000 \\ +110101 \\ \hline \mathbf{100001.001} \end{array}$$

[2 Marks]

b) Given the two-input OR gate expression $Y = A + B$

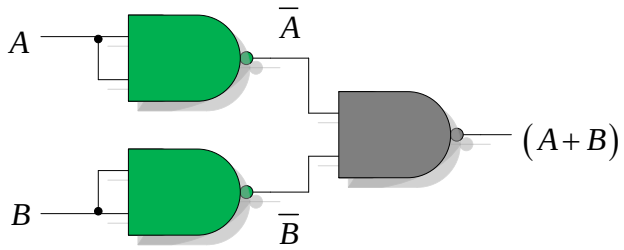
i) $Y = A + B = \overline{\overline{A}} + \overline{\overline{B}}$, by the Involution law,

It follows that $\overline{\overline{A}} + \overline{\overline{B}} = \overline{\overline{A} \cdot \overline{B}}$, by DeMorgan's theorem,

By the Idempotent law, $\overline{\overline{A} \cdot \overline{B}} = \overline{(\overline{A \cdot A}) \cdot (\overline{B \cdot B})}$.

Therefore, the modified form given as $Y = \overline{(\overline{A \cdot A}) \cdot (\overline{B \cdot B})}$ **[3 Marks]**

ii) Thus, the logic circuit is as shown below.



[3 Marks]

c) Given the POS expression $f(A,B,C,D) = \prod 0,2,5,7,8,10,13,15$

i) The expansion of the expression is of the form

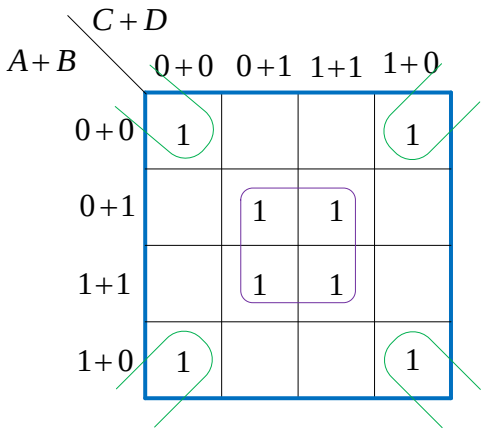
$$f(A,B,C,D) = \prod [(0+0+0+0),(0+0+1+0),(0+1+0+1),(0+1+1+1),$$
$$(1+0+0+0),(1+0+1+0),(1+1+0+1),(1+1+1+1)]$$

, or

$$f(A,B,C,D)=(A+B+C+D)\cdot(A+B+\overline{C}+D)\cdot(A+\overline{B}+C+\overline{D})\cdot(A+\overline{B}+\overline{C}+\overline{D})$$
$$\cdot(\overline{A}+B+C+D)\cdot(\overline{A}+B+\overline{C}+D)\cdot(\overline{A}+\overline{B}+C+\overline{D})\cdot(\overline{A}+\overline{B}+\overline{C}+\overline{D})$$

[3 Marks]

ii) The product of sums Karnaugh map is as shown below



Product-of-sums K-map

[4 Marks]

iii) Hence, the minimized Boolean expression is given by

$$f(A,B,C,D)=(B+D)\cdot(\overline{B}+\overline{D})$$

[2 Marks]

[Total 20 Marks]

QUESTION 4 [SOLUTION]

a) ECL has the following advantages over TTL (Pick any two):

- High switching speeds due to non-saturation of its transistors
- Low power noise due to small power swings during switching.
- Power supplies for ECL are easier to design due the almost constant power consumption.

[2 Marks]

ECL has the following disadvantages over TTL (Pick any two):

- Due to the fast switching and the constant power consumption, ECL consumes more power than TTL and is not ideal for mobile devices.
- ECL uses negative supply and therefore not easily mixed with other logic families.
- ECL has low noise margin and therefore susceptible to noise. **[2 Marks]**

b) The noise margin is given as

$$\begin{aligned} NM &= min\{LNM, HNM\} \\ &= min\{|V_{OL,Max} - V_{IL,Max}|, |V_{OH,Min} - V_{IH,Min}|\} \\ &= min\{|0.4 - 0.8|, |2.4 - 2.0|\} \\ &= min\{0.4\text{V}, 0.4\text{V}\} \\ &= 0.4\text{V} \end{aligned}$$

[6 Marks]

Noise Margin gives an indication of how much immunity the IC has to external stray voltages.

c) Conflicting design targets in ICs is Speed (Propagation delay) and Power. Therefore using these two parameters, the listed ICs have the following features:

- **7402**: Standard TTL with ordinary Speed and Power.
- **74H02**: High Speed TTL. By reducing internal resitances, the time constant is reduced and therefore increased switching time. With lower resistances, higher power dissipation.
- **74L02**: Low Power TTL. By increasing internal resistances, the time constant is increased and thus reduced currents, low power but slower switching speeds.
- **74LS02**: Low power Schottky TTL. By clamping the base-collector terminals with a Schottky diode, saturation of the transistors is avoided thus faster switching. This is the best compromise between speed and power.

[10 Marks]

[Total 20 Marks]

QUESTION 5 [SOLUTION]

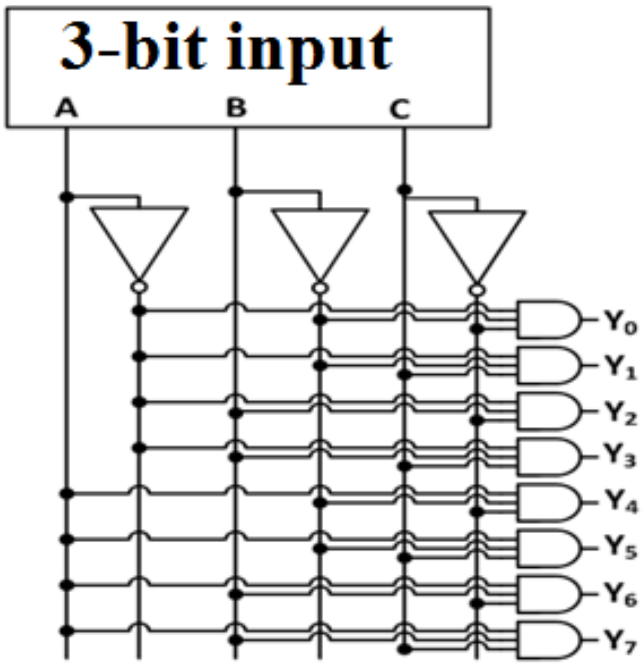
a)

i. The Truth Table requires that only 1 of the 8 outputs is HIGH for every 3-bit input:

ABC	OUTPUT ($Y_7 Y_6 Y_5 Y_4 Y_3 Y_2 Y_1 Y_0$)
000	00000001
001	00000010
010	00000100
011	00001000
100	00010000
101	00100000
110	01000000
111	10000000

[3 Marks]

ii. From the Truth Table above, the circuit implementation for the binary decoder is:



[4 Marks]

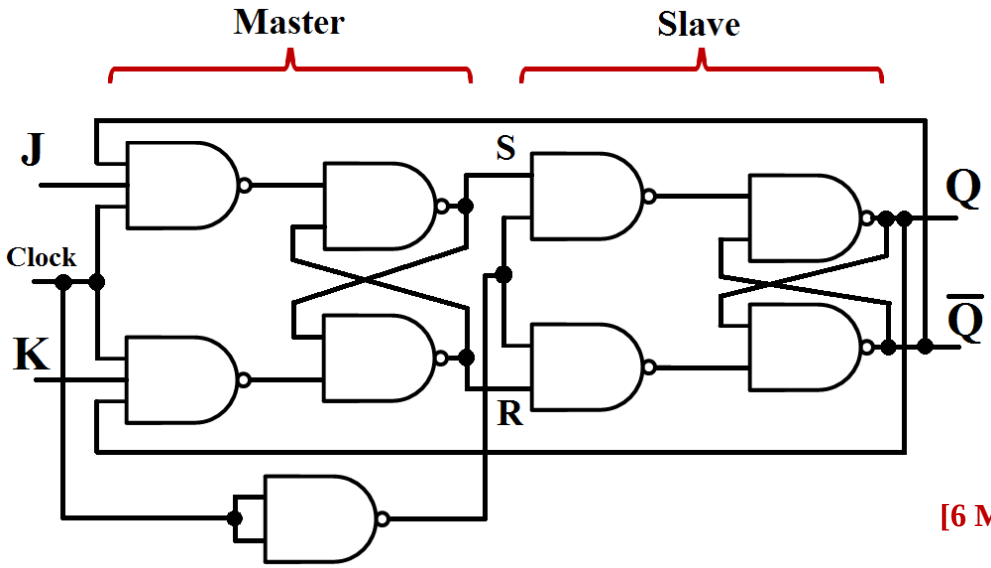
iii. Address decoding i.e. a given number of address bits selects only one memory location and keeps other memory locations off.

Also applied in binary-to-decimal decoding i.e. a binary number is fed through the register contents ABC and then the corresponding decimal location is activated.

[3 Marks]

b) For the JK Master-Slave Flip-flop:

i. Below is a NAND gate implementation of a JK Master-Slave Flip-flop



[6 Marks]

ii. The JK master-slave flip-flop has two sections, the master and the slave with clock signals that are complements of each other.

This means that when the clock is HIGH, the inputs J and K are latched into the master and do not affect the slave. When the clock goes LOW, the master is disabled and the slave takes the master's outputs for latching.

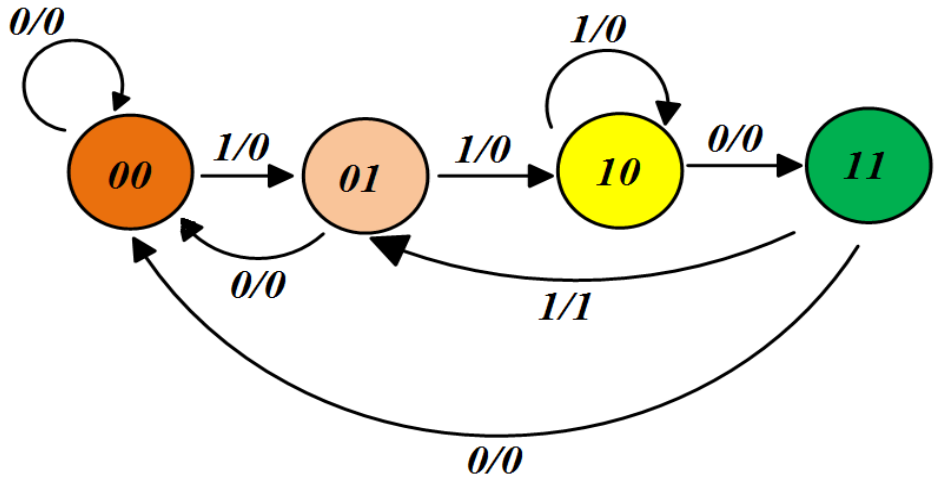
This prevents the slave's outputs from affecting the master when the clock width is larger than the propagation delay. This condition that is avoided is called the RACE-AROUND condition. The race-around condition produces unpredictable outputs.

[4 Marks]

[Total 20 Marks]

QUESTION 6 [SOLUTION]

a) Since the system is supposed to detect four bits (1101), the state transition diagram will need to have four states; the initial state will be for waiting for detection or fall back after detection the last bit. Four states require two bits to be fully represented. This is a Mealy machine and so input and output are on the transition arrows.



[4 Marks]

b) The state transition table will require two variables, A and B, to represent the state and a single variable, X, to represent the input.

Present State		Input	Next State		Output
A	***B***	***X***	***A***	***B***	***Y***
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	1	1	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	1	1

[6 Marks]

c) From the state transition table, we use the sum-of-products to relate the next state to the present state and the input and to also relate the output to the present state and the input. In the input equations below, NXT means next state and PRST means present state.

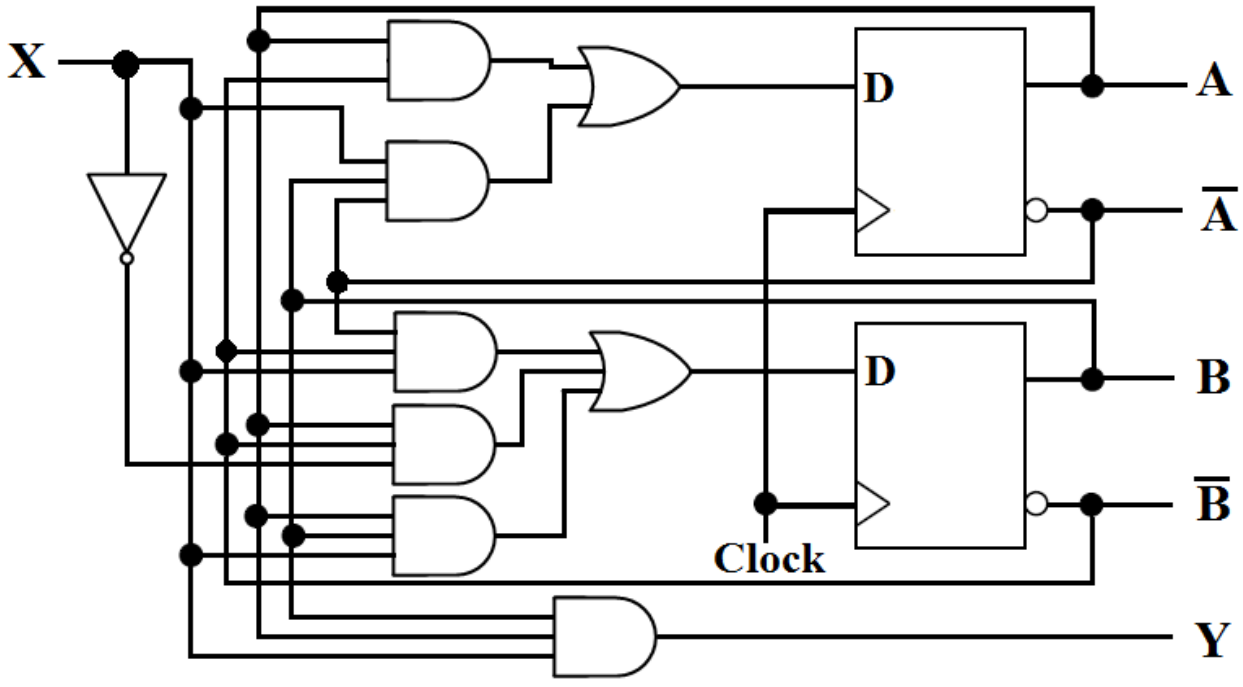
$$A_{NXT} = \overline{A}_{PRST} B_{PRST} X + A_{PRST} \overline{B}_{PRST} \overline{X} + A_{PRST} \overline{B}_{PRST} X$$
$$= \overline{A}_{PRST} B_{PRST} X + A_{PRST} \overline{B}_{PRST}$$

$$B_{NXT} = \overline{A}_{PRST} \overline{B}_{PRST} X + A_{PRST} \overline{B}_{PRST} \overline{X} + A_{PRST} B_{PRST} X$$

$$Y = A_{PRST} B_{PRST} X$$

[4 Marks]

d) Using the input equations above, the sequence detector logic circuit can be implemented as shown below:



[6 Marks]

[Total 20 Marks]

QUESTION 7 [SOLUTION]

a) The program counter contains the address of the instruction that will be executed in the next step. It is 16-bits. On the other hand, the stack pointer is a register that stores the value of the memory location in the stack (section of RAM) where the return addresses are stored to allow simple nesting of function calls in a program. **[4 Marks]**

b) The ALU in the 8085 microprocessor does among other functions the following operations:

- Addition: The assembly mnemonic is ADD.
- Subtraction: The assembly mnemonic is SUB.
- Logic OR: The assembly mnemonic is ORA.
- Logic AND: The assembly mnemonic is ANA.

[8 Marks]

c) In SAP, the adder has a controlled inverter on one of the two input bytes. This controlled inverter is implemented using XOR gates. Each two-input XOR gate takes in one of the bits from the byte that is to be subtracted. The other input to each XOR gate is a common SUB signal that also gets into the carry-in port of the LSB full adder. When the SUB signal is high, a 2's complement of the byte is fed into the adder/subtractor. When SUB is low, the byte passes to the adder/subtractor un-complemented. **[5 Marks]**

d) The Tri-state switches enable all the sections of the SAP computer to be able to share the W bus. When a sub-system's Tri-state switch is not enabled, the contents of that particular subsystem will not be available on the W bus and will therefore not interfere with other subsystems. When that subsystem's contents are required in another section of the computer, its tri-state switches will be enabled and its contents will then be available on the W bus.

[3 Marks]

[Total 20 Marks]

END OF EEE 3132 EXAM MODEL SOLUTIONS