

QUESTION 1 [SOLUTION]

a) ECL has the following advantages over TTL (Pick any two):

- High switching speeds due to non-saturation of its transistors
- Low power noise due to small power swings during switching.
- Power supplies for ECL are easier to design due the almost constant power consumption.

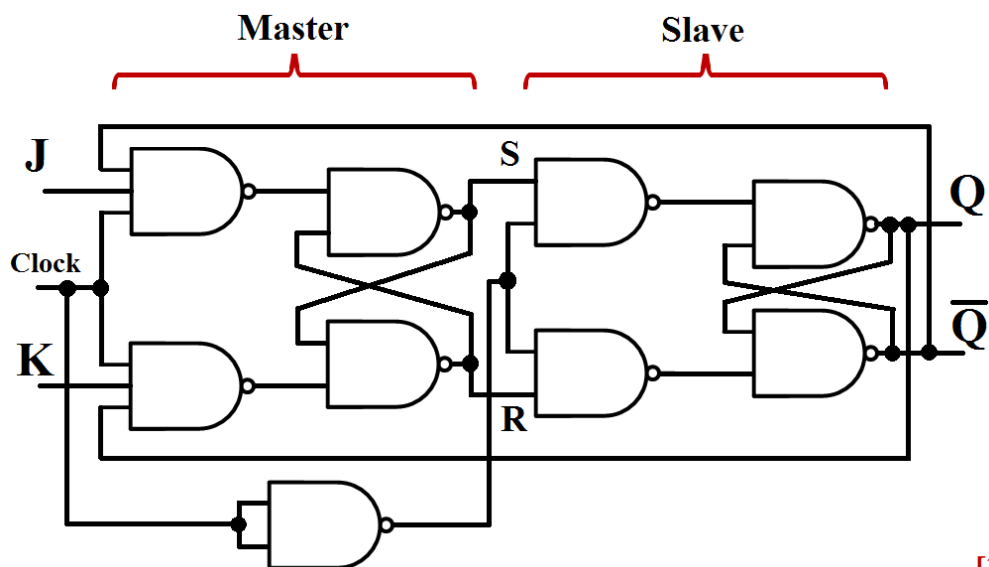
[2 Marks]

ECL has the following disadvantages over TTL (Pick any two):

- Due to the fast switching and the constant power consumption, ECL consumes more power than TTL and is not ideal for mobile devices.
- ECL uses negative supply and therefore not easily mixed with other logic families.
- ECL has low noise margin and therefore susceptible to noise.

[2 Marks]

b) Below is a JK Master-Slave flip flop:



[3 Marks]

The JK master-slave flip-flop has two sections, the master and the slave with clock signals that are complements of each other.

This means that when the clock is HIGH, the inputs J and K are latched into the master and do not affect the slave. When the clock goes LOW, the master is disabled and the slave takes the master's outputs for latching.

This prevents the slave's outputs from affecting the master when the clock width is larger than the propagation delay. This condition that is avoided is called the RACE-AROUND condition. The race-around condition produces unpredictable outputs.

[3 Marks]

c) Conflicting design targets in ICs is Speed (Propagation delay) and Power. Therefore using these two parameters, the listed ICs have the following features:

- **7402:** Standard TTL with ordinary Speed and Power.
- **74H02:** High Speed TTL. By reducing internal resistances, the time constant is reduced and therefore increased switching time. With lower resistances, higher power dissipation.
- **74L02:** Low Power TTL. By increasing internal resistances, the time constant is increased and thus reduced currents, low power but slower switching speeds.
- **74LS02:** Low power Schottky TTL. By clamping the base-collector terminals with a Schottky diode, saturation of the transistors is avoided thus faster switching. This is the best compromise between speed and power.

[10 Marks]

[Total 20 Marks]

QUESTION 2 [SOLUTION]

- a) The timing circuit is an accurate clock generator that uses a crystal oscillator to generate a 1MHz clock signal. The clock signal is then divided by 10^6 to create a 1Hz clock signal. The 1Hz signal will drive the JK flip flop and the output of the flip flop will be a 0.5Hz signal, i.e. the output will be high for 1 second. This high output will then drive the AND gate. The number of pulses from the zero-crossing detector will pass through the AND gate and will

be counted by the binary counter. The number on the counter is the number of pulses in a second and this will be the frequency of the input signal in hertz.

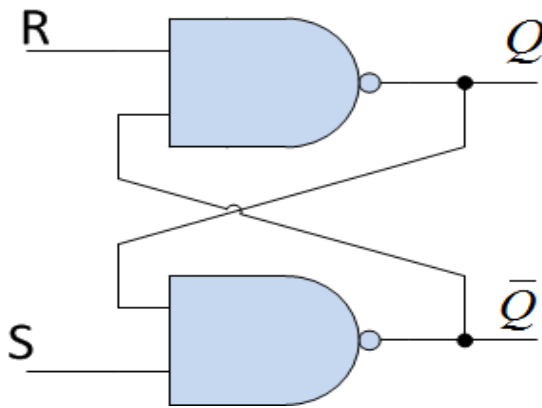
[10 Marks]

b)

- i. **EPROM** – Erasable Programmable Read Only Memory
EEPROM – Electrically Erasable Programmable Read Only Memory
- ii. EPROM is electrically programmed by the user and can be erased by using ultraviolet light. EEPROM just like EPROM is electrically programmable but is also electrically erasable; this is done with the EEPROM still in the system.
- iii. Due to the fact that EEPROM can be erased whilst still in the circuit, it has the advantage over EPROM in that it reduces erasure procedures and does not need additional special tools like UV system.

[5 Marks]

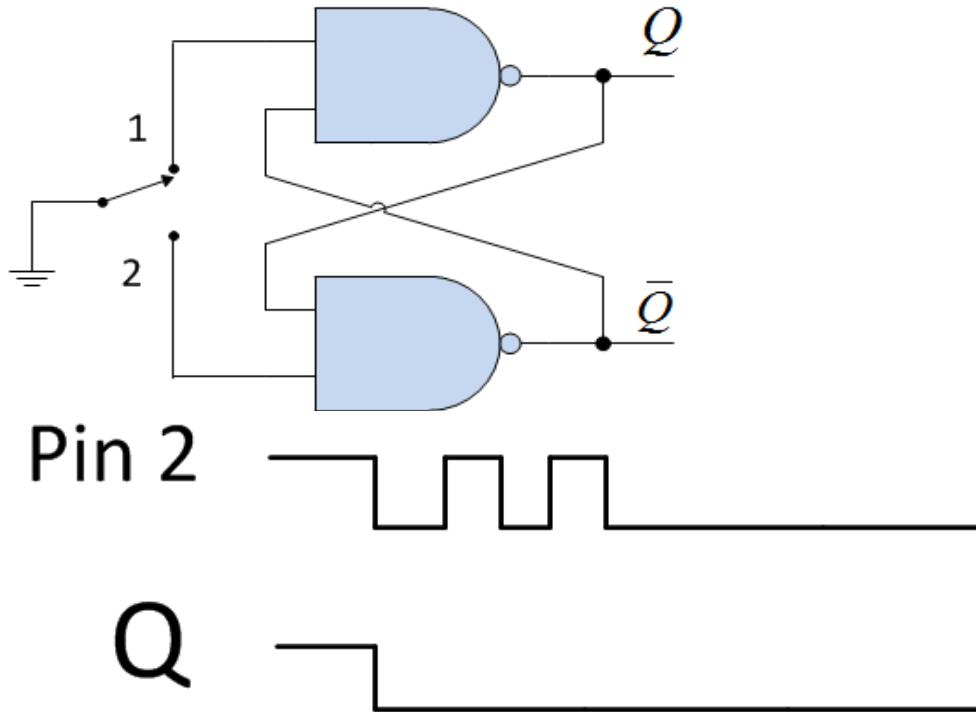
c) Below is a NAND SR latch and the associated truth table



R	S	Y	Comments
0	0	**	Race Conditions
0	1	1	Set
1	0	0	Reset
1	1	NC	No Change

[2 Marks]

The output of the RS latch once set maintains its state until the reset signal is high. Once set (or reset), the output stays high (or low) regardless of the set signal (or reset) going low. Since mechanical switches bounce when moved to the closed position, the above feature of RS latches can be used to de-bounce switches because as the switch makes and breaks, the output of the latch will not change and this therefore eliminates the effects of switch bouncing as shown below when switch is moved from position 1 to position 2:



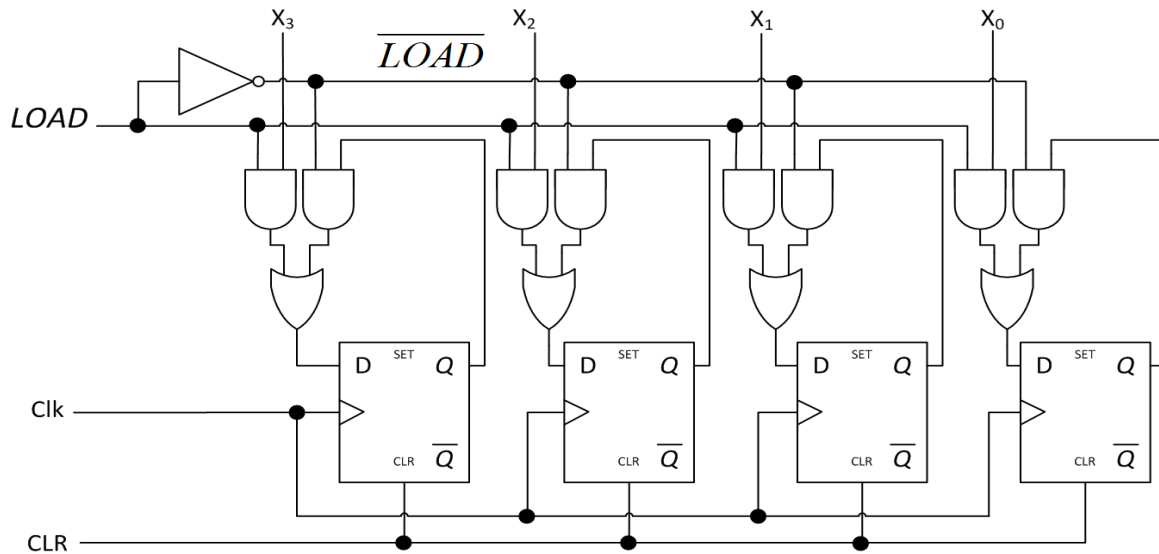
[3 Marks]

[Total 20 Marks]

QUESTION 3 [SOLUTION]

- The program counter contains the address of the instruction that will be executed in the next step. It is 16-bits. On the other hand, the stack pointer is a register that stores the value of the memory location in the stack (section of RAM) where the return addresses are stored to allow simple nesting of function calls in a program. [4 Marks]
- To turn the simple buffer register into a controlled buffer register, we add a two-input AND gate at the input, one for each bit, and so each input bit will be AND-ed with a control signal we shall call LOAD. This means that the data from the input will only be passed to the flip

flops if the LOAD signal is high. To maintain or refresh the stored data, we will use another two-input AND gate for each bit but this time the two inputs to this AND gate will be the output of each flip flop and the inverse of the LOAD signal. This is shown in the figure below:



[8 Marks]

c) Binary counters find applications in **Frequency measurements, time measurements, distance measurements** and **speed measurements**.

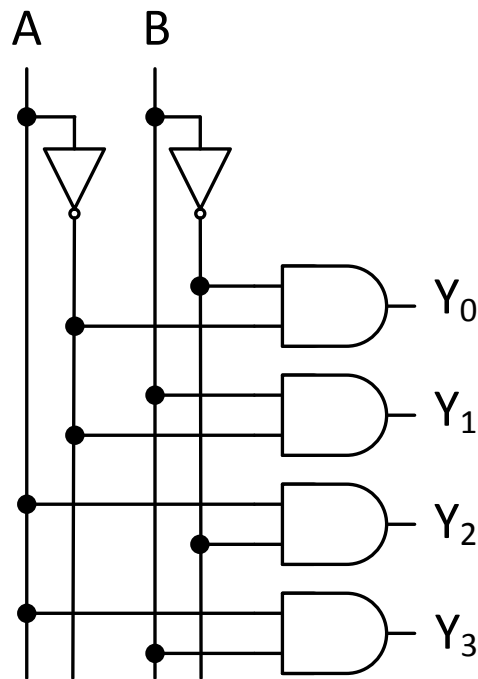
[2 Marks]

d) A binary decoder has digital input (a binary word) and only one of the many lines is high at a time. This relationship between input and output is shown in the truth table below:

A	B	Y ₃	Y ₂	Y ₁	Y ₀
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

[1 Marks]

Using the truth table above with A and B as the inputs and Y_3 , Y_2 , Y_1 and Y_0 as output, the logic circuit implementation is shown below:



[1 Marks]

The above decoder finds applications in address decoding for digital storage. The inputs A and B represent an address and the outputs Y_3 , Y_2 , Y_1 , Y_0 are connected to the word-line (memory locations). This means that a single address will only activate a specific memory location.

[1 Marks]

- e) The first first line, labeled “Start”, will load register C with the value F (Hex) or 15 in decimal. Then the second line, labeled “Again”, will decrement the contents of register C by one. The third line will check for the zero flag and will go back to second line if the value in register C is not zero. This means that the code will just count down from 15 and will only stop when contents of register C is zero. The display on the screen will therefore be 15,14,13,12,11, 10, 9, 8, 7, 6,5, 4, 3, 2, 1, 0.

[3 Marks]

[Total 20 Marks]

QUESTION 4 [SOLUTION]

a)

i) To perform the addition $(AF1.B3)_{16} + (FFF.E)_{16}$, we first convert the hexadecimal numbers into the binary equivalents, that is:

$$(AF1.B3)_{16} = 101011110001.10110011_2, \text{ and}$$

$(FFF.E)_{16} = 111111111111.11100000_2$, with four zeros appended at the end for balance summation.

$$\begin{array}{r} 101011110001.10110011 \\ + 111111111111.11100000 \\ \hline \mathbf{1101011110001.10010011} \end{array},$$

Converting the sum to hexadecimal yields, $(AF1.B3)_{16} + (FFF.E)_{16} = (\mathbf{1AF1.93})_{16}$

[5 Marks]

ii) The decimal number 325.125_{10} is converted to its binary equivalent by converting whole and fractional numbers as shown below:

2	325	remainder
	162	1
	81	0
	40	1
	20	0
	10	0
	5	0
	2	1
	1	0
	0	1

	Product	Carry
2×0.125	0.25	0
2×0.25	0.5	0
2×0.5	1.0	1

Therefore, $325.125_{10} = \mathbf{101000101.001}_2$

[3 Marks]

b) Analysis of the Spacecraft triple sensing system yields :

i) The truth-table for the spacecraft triple sensing system, taking **0** to denote ‘no action’ and **1** to denote ‘action’ is given as

Truth-table

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

[3 Marks]

- ii) From the truth table the minterm (sum-of-products) Boolean expression is given by

$$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

[2 Marks]

- iii) Using the Karnaugh map method Boolean expression is simplified as

	BC	00	01	11	10
A	0			1	
	1		1	1	1

Based on the K-map the simplified expression is $Y = AB + AC + BC$

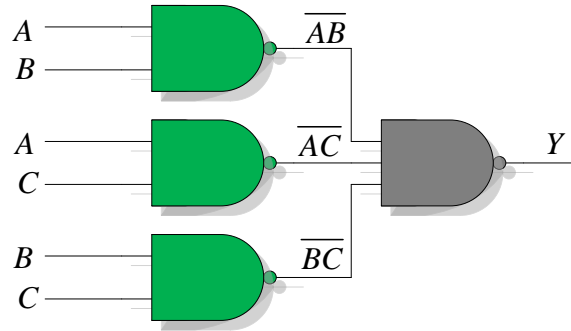
[3 Marks]

- iv) By DeMorgan's theorem, $\overline{\overline{AB} \cdot \overline{AC} \cdot \overline{BC}} = \overline{\overline{AB}} + \overline{\overline{AC}} + \overline{\overline{BC}} = AB + AC + BC$, thus,

$$Y = AB + AC + BC = \overline{\overline{AB} \cdot \overline{AC} \cdot \overline{BC}}.$$

[2 Marks]

- v) Finally the logic circuit for the expression obtained in (iv) is as shown below.



[2 Marks]

[Total 20 Marks]

QUESTION 5 [SOLUTION]

- a) In signed 2's complement, the we perform the following
 i) The 8 bit 2's complement notation of +15 and -78 are obtained as follows,

2	15	remainder
	7	1
	3	1
	1	1
	0	1

2	78	remainder
	39	0
	19	1
	9	1
	4	1
	2	0
	1	0
	0	1

Therefore, $(15)_{10} = \mathbf{00001111}$ in 8 bit 2's complement notation. [1 Mark]

Similarly, $78_{10} = 01001110_2$, whose 1's complement is 10110001. Finally, the 2's complement is $10110001 + 1 = 10110010$.

Therefore, $-78_{10} = \mathbf{10110010}_2$ in 8 bit 2's complement notation. [2 Marks]

- ii) Hence, the 2's complement arithmetic operation $(15)_{10} - (78)_{10}$ is performed as follows:

<u>2's compl</u>	<u>1's compl</u>
00001111	11000001
+ 10110010	- 1
11000001	11000000

Since there is no carry, and the MSB is 1, the answer is presumably negative. Thus, the 1's complement is found as shown above. Finally, the actual magnitude is obtained by taking the 1's complement of **11000000**.

Therefore, the actual magnitude is $-\mathbf{00111111}$ [3 Marks]

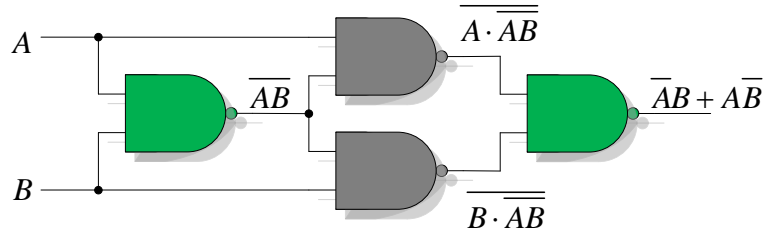
- b)
 i) Given the EX-OR expression $F = \bar{A}B + A\bar{B}$, it follows that,

$$F = \overline{\overline{\overline{AB}} + \overline{\overline{\overline{AB}}}} = \overline{\overline{\overline{AB}} + \overline{\overline{\overline{AB}}}} \quad \text{by the Involution law.}$$

$$F = \overline{\overline{\overline{A \cdot B}} \cdot \overline{\overline{\overline{A \cdot B}}}} \quad \text{by DeMorgan's law.}$$

$$\text{Therefore, } F = \overline{\overline{\overline{B \cdot (\overline{A+B})}} \cdot \overline{\overline{\overline{A \cdot (\overline{A+B})}}}} = \overline{\overline{\overline{B \cdot A \cdot \overline{B}}} \cdot \overline{\overline{\overline{A \cdot A \cdot \overline{B}}}}} \quad \text{[4 Marks]}$$

ii) The circuit implementation is thus as shown below.



[2 Marks]

c) Given the POS expression $f(A, B, C, D) = \prod 0, 2, 5, 7, 8, 10, 13, 15$

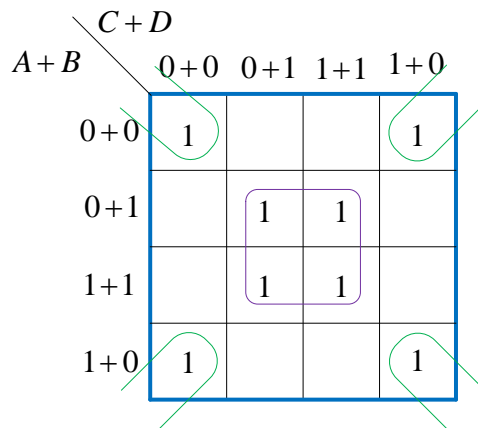
i) The expansion of the expression is of the form

$$f(A, B, C, D) = \prod [(0+0+0+0), (0+0+1+0), (0+1+0+1), (0+1+1+1), (1+0+0+0), (1+0+1+0), (1+1+0+1), (1+1+1+1)] \quad \text{, or}$$

$$f(A, B, C, D) = (A+B+C+D) \cdot (A+B+\overline{C}+D) \cdot (A+\overline{B}+C+\overline{D}) \cdot (A+\overline{B}+\overline{C}+\overline{D}) \cdot (\overline{A}+B+C+D) \cdot (\overline{A}+B+\overline{C}+D) \cdot (\overline{A}+\overline{B}+C+\overline{D}) \cdot (\overline{A}+\overline{B}+\overline{C}+\overline{D})$$

[2 Marks]

ii) The product of sums Karnaugh map is as shown below



[4 Marks]

Product-of-sums K-map

iii) Hence, the minimized Boolean expression is given by

$$f(A, B, C, D) = (B+D) \cdot (\overline{B}+\overline{D}) \quad \text{[2 Marks]}$$

[Total 20 Marks]

QUESTION 6 [SOLUTION]

- a) Conversion to 8 bit Excess-3 codes is achieved as follows:
 i) Since, $15_{10} = 0015_{10}$, adding 3 to each digit yields '3', '3', '4', and '8' which when converted to their binary equivalents gives the Excess-3 code, i.e.,

$$15_{10} = \mathbf{0011\ 0011\ 0100\ 1000} \text{ in Excess-3 code.} \quad [1.5 \text{ Marks}]$$

Similarly, $671_{10} = 0671_{10}$, adding 3 to each digit yields '3', '9', '10', and '4' which when converted to their binary equivalents gives the Excess-3 code, i.e.,

$$671_{10} = \mathbf{0011\ 1001\ 1010\ 0100} \text{ in Excess-3 code.} \quad [1.5 \text{ Marks}]$$

- ii) To Evaluate $(111.001)_2 \times (1.11)_2$ correct to two binary places, we have

$$\begin{array}{r} 111.001 \\ \times \quad 1.11 \\ \hline 111001 \\ 111001 \\ 111001 \\ \hline \mathbf{1100.0111} \end{array}$$

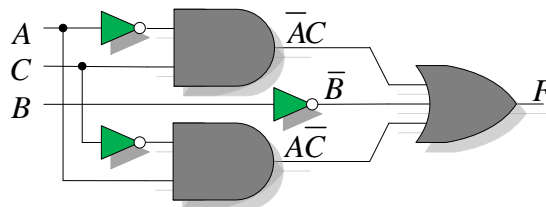
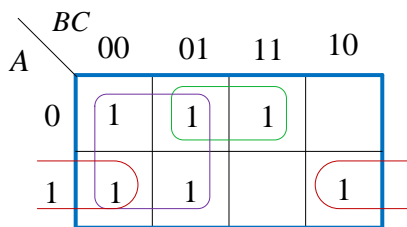
Thus, $(111.001)_2 \times (1.11)_2 = \mathbf{1100.01}_2$ correct to two binary places. [2 Marks]

- b) The simplification using K-maps is done as follows:

- i) First of all we express $F = A\bar{B} + \bar{A}\bar{B} + ABC\bar{C} + \bar{A}BC$ in canonical form before simplifying it using the K-map. That is,

$$F = A\bar{B}(C + \bar{C}) + \bar{A}\bar{B}(C + \bar{C}) + ABC\bar{C} + \bar{A}BC$$

$F = A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + ABC\bar{C} + \bar{A}BC$. It follows that the Karnaugh map is of the form,

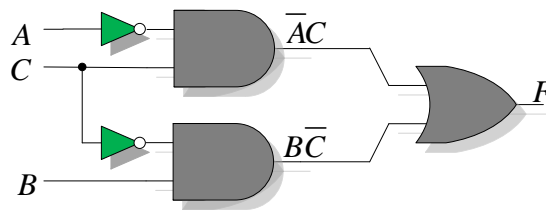
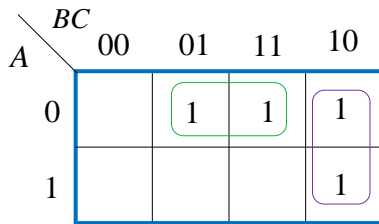


Therefore, the simplified expression is, $F = \bar{B} + \bar{A}C + A\bar{C}$, the circuit implementation of which is as shown above. [3 Marks]

- ii) Expressed in canonical form, $F = \bar{A}C + B\bar{C} + \bar{A}B$ is as shown:

$$F = \bar{A}C(B + \bar{B}) + B\bar{C}(A + \bar{A}) + \bar{A}B(C + \bar{C}), \text{ that is to say,}$$

$F = \bar{A}BC + \bar{A}\bar{B}C + A\bar{B}C + \bar{A}\bar{B}\bar{C} + \bar{A}BC + \bar{A}\bar{B}\bar{C}$. It follows that the Karnaugh map is of the form,



Therefore, the simplified expression is $F = \bar{A}C + B\bar{C}$, the circuit implementation of which is as shown above. [3 Marks]

c)

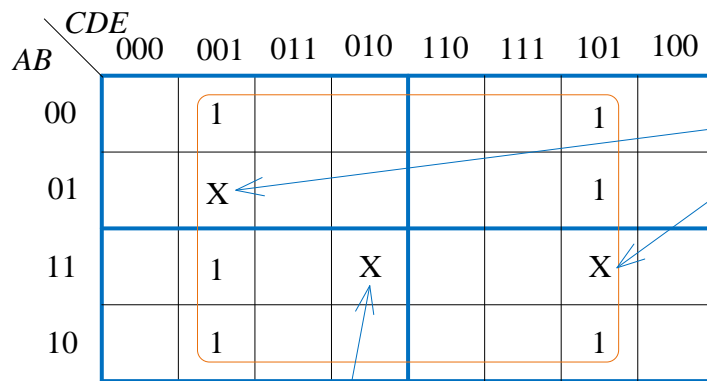
i) Given SOP Boolean expression in short form notation as

$$f(A, B, C, D, E) = \sum 1, 5, 13, 17, 21, 25 + \sum_d 9, 26, 29, \text{ its expanded form is as shown}$$

$$f(A, B, C, D, E) = \sum [00001, 00101, 01101, 10001, 10101, 11001] + \sum_d [01001, 11010, 11101]$$

[3 Marks]

Thus, the Karnaugh map is as shown:



Take these don't cares to be 1's

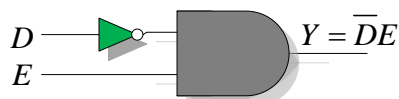
[3 Marks]

Take this don't care to be a 0

ii) From the Karnaugh map only one group is formed, thus the simplified expression is given by,

$$f(A, B, C, D, E) = \bar{D}E \quad \text{[2 Marks]}$$

iii) Consequently, the minimized logic circuit is found to be



[1 Mark]

[Total 20 Marks]

END OF EEE 3131 EXAM MODEL SOLUTIONS