EEE 3131 – DIGITAL ELECTRONICS
MODEL SOLUTIONS TO MID YEAR EXAMINATION - 2015/2016 ACADEMIC YEAR
DATE OF EXAMINATION: MAY, 2016

QUESTION 1 [SOLUTION]

a)

a) 7400 – Standard TTL with median values for speed and power consumption **[2 Marks]**

b) 74H00 – This is High Speed TTL. The high speed is achieved by reducing the internal resistances of the standard TTL. The reduced resistance reduces the time constant and therefore reduced propagation delay in the IC. With a reduction in resistance but at the same voltage levels, more current is drawn by 74H00 series and therefore in gaining speed, power consumption also increases. **[3 Marks]**

c) 74L00 – This is Low Power TTL. The internal resistances of standard TTL are increased at the same value of voltage and thus reduced power consumption. This increases the RC time constant and so the 74L00 series is power efficient but relatively slower than 74H00 series. **[3 Marks]**

d) 74S00 – This is Schottky TTL. Implemented by using a Schottky diode to clamp the collector-base junction of a transistor, i.e. anode on base and cathode on the collector: this forms a Schottky transistor. This configuration limits V_{CE} and so prevents the transistor from going into saturation, thus relatively faster switching times – slightly faster than 74H00. **[3 Marks]**

b)

i) The fan-out is given by $FO = \min\left\{\frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}}\right\} \Rightarrow \min\left\{\frac{400\mu A}{80\mu A}, \frac{16mA}{1.6mA}\right\} = 5$

The fan-out of five indicates that only five AND gates of the above specs can be connected on the output of one of the AND gates without causing damage due to overcurrent. **[4 Marks]**

ii) To find the maximum allowable interference voltage, we need to calculate the noise margin i.e. $NM = \min\{HNM, LNM\}$, where $HNM = 2.4\text{V} - 2.0\text{V} = 0.4\text{V}$ and $LNM = 0.8\text{V} - 0.4\text{V} = 0.4\text{V}$. The noise margin is therefore 0.4V and the implication is

that the maximum noise voltage that can be added onto the input signal without causing undesirable output is $0.4V$. **[5 Marks]**

[Total 20 Marks]

QUESTION 2 [SOLUTION]

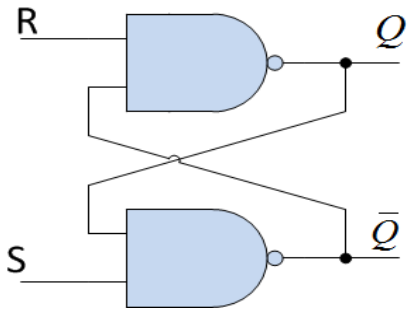
a) Considering EPROM and EEPROM,

i) EPROM stands for Erasable Programmable Read Only Memory and EEPROM stands for Electrically Erasable Programmable Read Only Memory. **[2 Marks]**

ii) The two main differences are that EPROM requires UV light to erase its contents while EEPROM uses electric signals to erase. The second difference is that the erasing of EPROM is clears the entire chip while EEPROM can be erased byte-by-byte. **[2 Marks]**

iii) EEPROM has the advantage that it can be erased in-circuit and does not require specialized hardware for the erasing process while EPROM requires that the chip is removed and put in a UV drawer, specialized equipment for erasure. **[2 Marks]**

b) Below is a NAND SR latch and the associated truth table



[2 Marks]

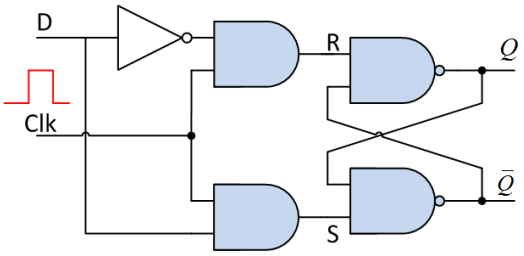
R	S	Y	Comments
0	0	**	Race Conditions
0	1	1	Set
1	0	0	Reset
1	1	NC	No Change

[1 Mark]

c) The disadvantage of the NAND SR-latch above is that when the inputs are R = S = 0, the state of the flip-flop will be unpredictable due to the race condition. This is prevented by converting it to a clocked D-flip flop. This is done by using two NAND gates at the input of the NAND SR flip-flop and then using an inverter before one of the AND gates at the input.

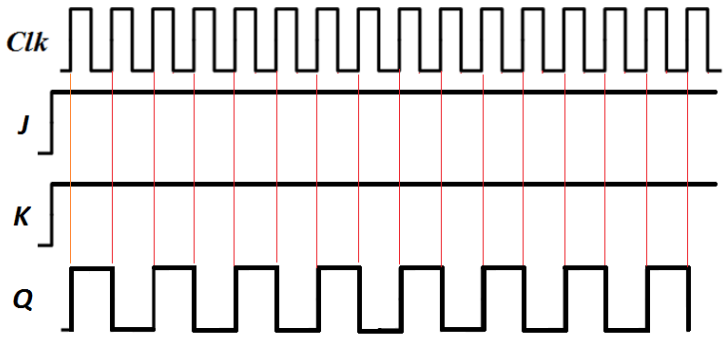
[2 Marks]

The implementation of the level-triggered D-flip-flop is shown below for the level triggered clocked D-flip-flop:



[3 Marks]

d) The timing diagram for the JK flip-flop is shown below:



[4 Marks]

e) The JK master-slave flip-flop has two sections, the master and the slave. The clock signals to the two sections are such that they are complements of each other. This means that when the clock is HIGH, the inputs J and K are latched into the master and do not affect the slave. When the clock goes LOW, the master is disabled and the slave takes the master's outputs for latching.

This prevents the slave's outputs from affecting the master when the clock width is larger than the propagation delay. This condition that is avoided is called the RACE-AROUND condition. The race-around condition produces unpredictable outputs. **[2 Marks]**

[Total 20 Marks]

QUESTION 3 [SOLUTION]

a)

i) A microprocessor is simply a central processing unit on a chip. It is only capable of processing and lacks the peripherals. A microcontroller on the other hand has the central processing unit as well as the peripherals like ADC, PWM, counters, I/O, memory, etc.

[2 Marks]

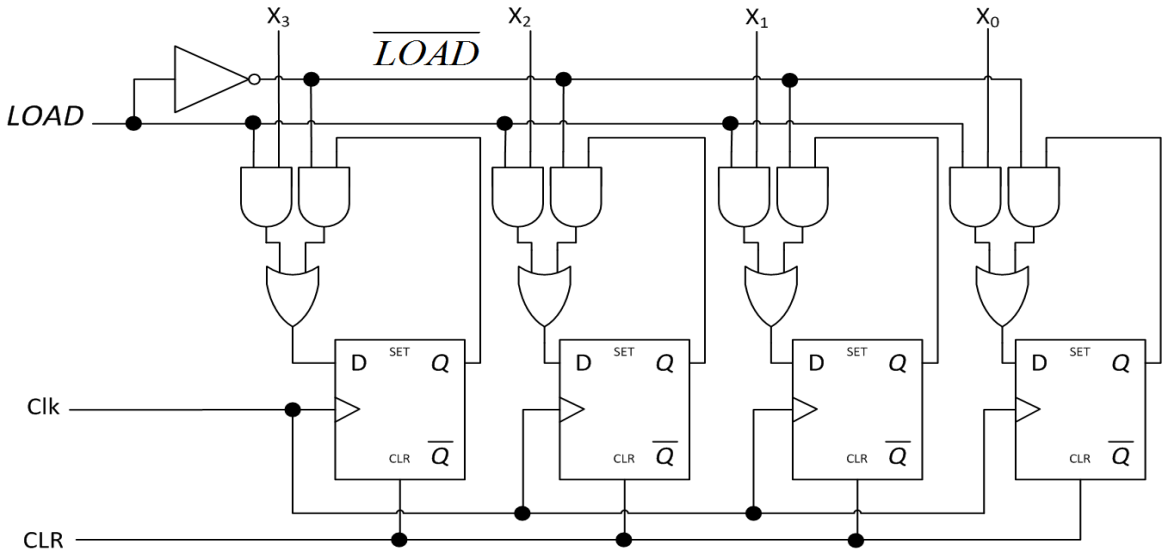
ii) Atmel's AVR Microcontrollers (Atmega, ATTiny, etc) and Microchip's PIC microcontrollers.

[2 Marks]

b) To turn the simple buffer register into a controlled buffer register, we add a two-input AND gate at the input, one for each bit, and so each input bit will be AND-ed with a control signal we shall call LOAD. This means that the data from the input will only be passed to the flip flops if the LOAD signal is high. To maintain or refresh the stored data, we will use another two-input AND gate for each bit but this time the two inputs to this AND gate will be the output of each flip flop and the inverse of the LOAD signal.

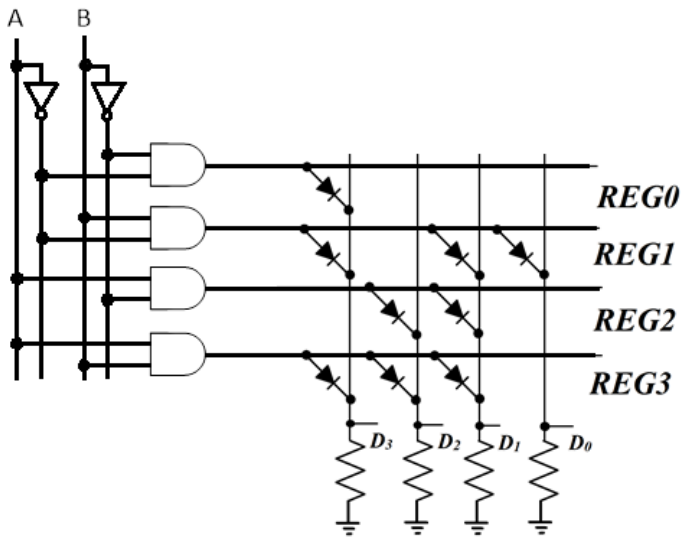
[4 Marks]

The logic circuit is shown in the figure below:



[6 Marks]

c) A binary decoder would be an alternative way of addressing the memory locations in the ROM. The complete design is shown below. The memory locations will be accessed by using AB as the address lines:



[6 Marks]

[Total 20 Marks]

QUESTION 4 [SOLUTION]

a)

i) The minimum number of flip-flops, n, required for a MOD-K binary counter is determined by finding the logarithm to base two of K i.e. $n = \log_2 K$. So in this case, $K = 32$. This means that the minimum number of flip-flops required for a MOD-32 counter is $n = \log_2 32 = 5$. **[2 Marks]**

ii) The terminal count, j, in a counter that uses n flip-flops is given by $j = 2^n - 1$. In this case, the counter in question uses five flip-flops, i.e. $n = 5$. This means that the terminal count is $j = 2^5 - 1 = 31$. The counter will count 31 clock pulses before resetting to zero.

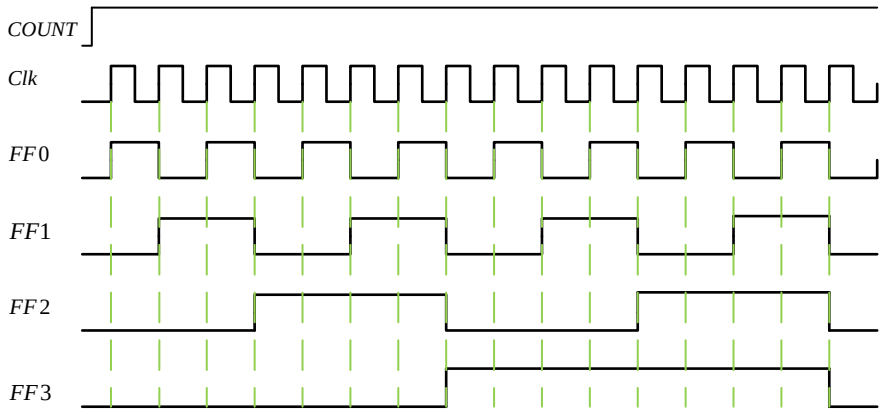
[1 Marks]

iii) A MOD-16 synchronous counter will use four flip-flops and will reset to zero after the fifteenth pulse and restart the count. The state table is shown below:

clock Pulse #	*Count Value*
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

So with the current state of the counter at 1000_2, counting 20 clock pulses through the table will give the final state as 1100_2. **[2 Marks]**

b) Below is the timing diagram for the synchronous 4-bit counter:



[10 Marks]

c)

i) The three kinds of buses found in a computer are

Data Bus: Carrying the actual data bits. **[1 Mark]**

|Address Bus: This carries the address to the address decoder. **[1 Mark]**

Control Bus: This carries the control signals from the instruction decoder. **[1 Mark]**

ii) With a 16-bit address bus, the maximum number of memory locations that can be addressed is given by raising two to the power equal to the bus size, i.e.

$$\#\ of\ \ locations = 2^{16} = 65,536$$ **[2 Marks]**

[20 Marks]

QUESTION 5 [SOLUTION]

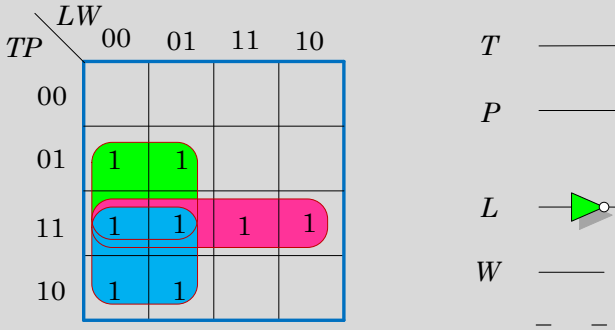
(a) First, write in Boolean equation form the conditions that will activate the alarm:

$$\text{alarm} = LTP + \overline{L}TW + \overline{L}\,\overline{T}P + \overline{L}\overline{W}T$$

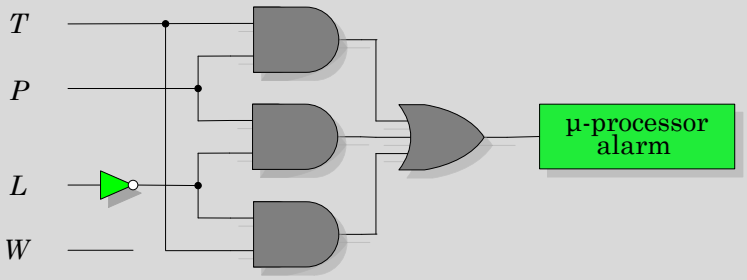
Next, we express the Boolean expression in canonical form for the purpose of mapping on the Karnaugh map, i.e.,

$$\text{alarm} = TPLW + TPL\overline{W} + TP\overline{L}W + T\overline{P}\,\overline{L}W + \overline{T}P\overline{L}W + \overline{T}P\overline{L}\,\overline{W} + TP\overline{L}\,\overline{W} + T\overline{P}L\overline{W}.$$

Thus, the Karnaugh map and implementation design are shown below.



(a) Karnaugh map



Alarm = $TP + P\overline{L} + T\overline{L}$

(b) Circuit implementation

[4 Marks]

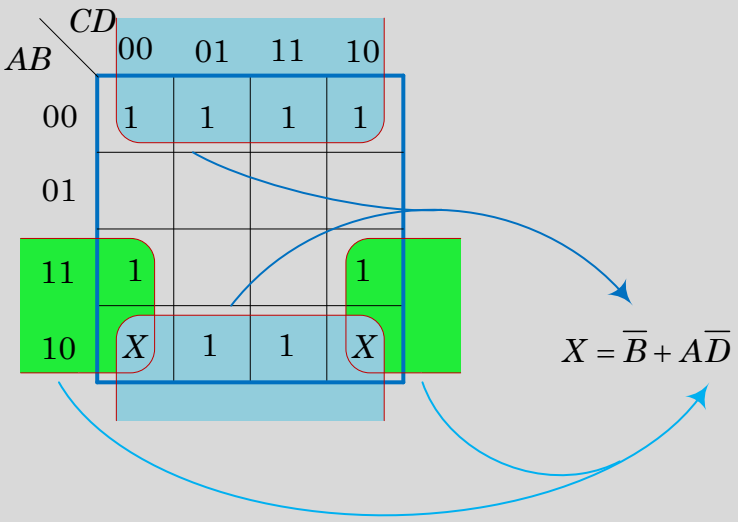
[4 Marks]

(b) For the given Boolean expression:

(i) Since $f(A,B,C,D) = \sum 0,1,2,3,9,11,12,14 + \sum_d 8,10$ in compact form, the expanded expression is of the form,

$$f(A,B,C,D) = \sum[0000,\ 0001,\ 0010,\ 0011,\ 1001,\ 1011,\ 1100,\ 1110] + \sum_d[1000,\ 1010]$$ **[2 Marks]**

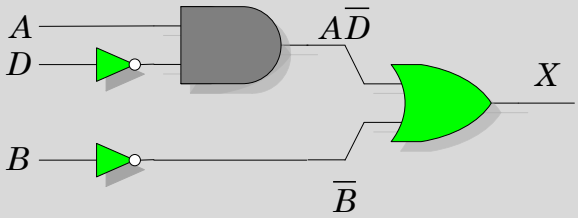
Thus, the Karnaugh map is of the form:



[6 Marks]

(ii) The simplified expression is thus, $f(A,B,C,D) = \overline{B} + A\overline{D}$. **[2 Marks]**

(iii) The minimized logic circuit is as shown too.

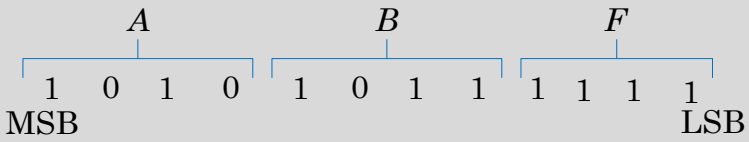


[2 Marks]

[Total 20 Marks]

QUESTION 6 [SOLUTION]

(a) To convert the Hexadecimal number $\mathrm{ABF\,H}$ to Gray code, we first convert the number to it's binary equivalent, i.e.;



The Gray code equivalent is thus found as follows:

Step 1: MSB is the same as that of binary number.

Step 2: Second MSB is found by adding MSB and 2nd MSB in the binary number ignoring the carry.

Step 3: Third MSB is found by adding 2nd MSB and 3rd MSB in the binary number, ignoring carry.

Step 4: The procedure is repeated until all bits have been exhausted.

Thus, $ABF_{16} = \mathbf{111111100000}\ \mathrm{Gray\ Code}$. **[3 Marks]**

(b) In signed 2's complement, the we perform the following

(i) The 8 bit 2's complement notation of $+42$ and -23 are obtained as follows,

2	42	remainder
	21	0
	10	1
	5	0
	2	1
	1	0
	0	1

2	23	remainder
	11	1
	5	1
	2	1
	1	0
	0	1

Therefore, $(42)_{10} = \mathbf{00101010}$ in 8 bit 2's complement notation. **[1 Mark]**

Similarly to regular binary, $23_{10} = \mathbf{00010111}_2$, whose 1's complement is 11101000. Finally, the 2's complement is $11101000 + 1 = 11101001$.

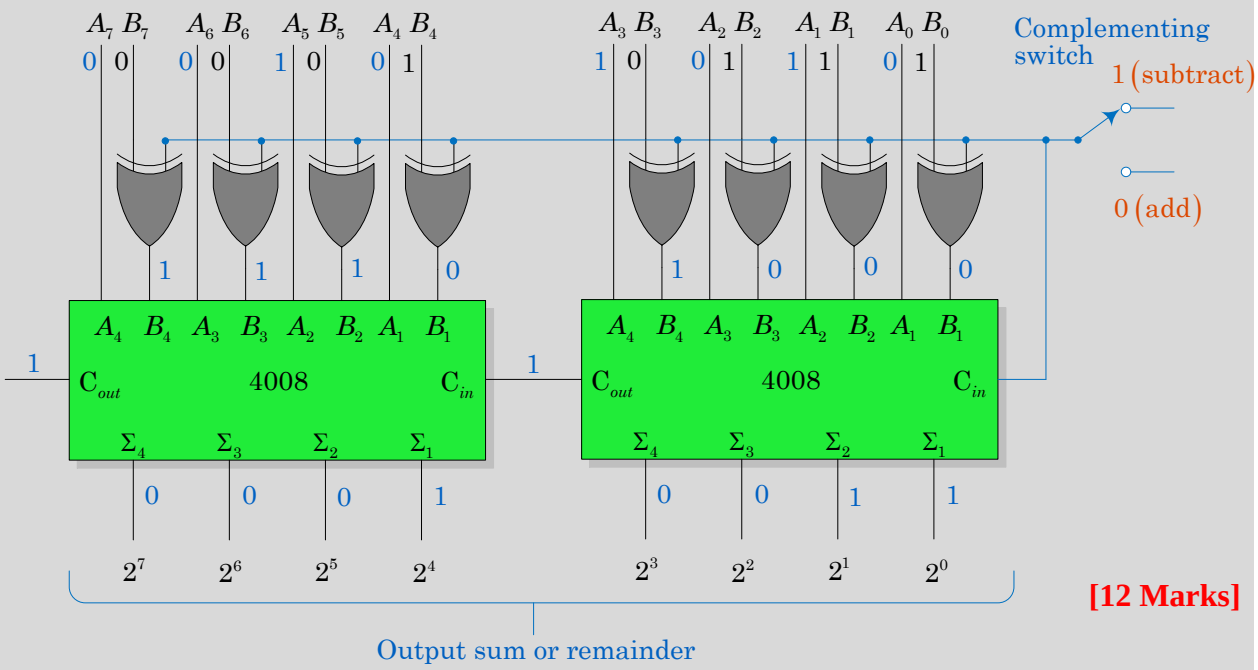
Therefore, $-23_{10} = \mathbf{11101001}_2$ in 8 bit 2's complement notation. **[2 Marks]**

(ii) Hence, the 2's complement arithmetic operation $(42)_{10} - (23)_{10}$ is performed as follows:

$$\begin{array}{r} \text{2's compl} \\ \mathbf{00101010} \\ +\mathbf{11101001} \\ \hline \mathbf{100010011} \end{array}$$

Since there is a carry we ignore the it and the MSB is certainly 0. Thus, the answer is positive and it magnitude is **00010011**. **[2 Marks]**

(c) The design of a 2's complement binary adder/subtracter which adds two 8-bit binary words is as shown:



[12 Marks]

[Total 20 Marks]

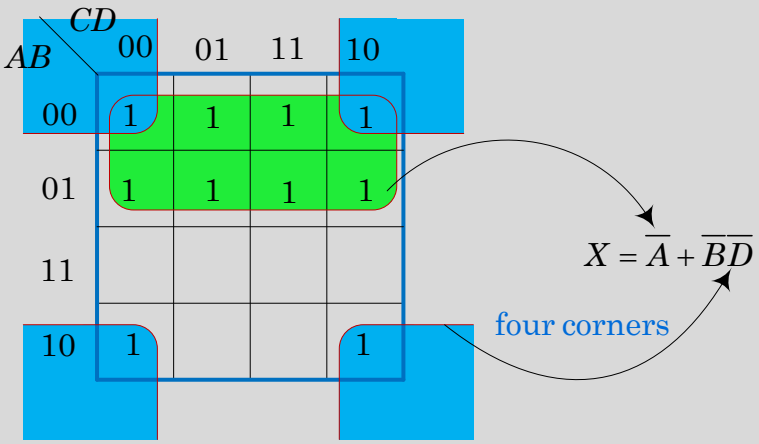
QUESTION 7 [SOLUTION]

(a) Given the expression $X = \overline{A}\overline{D} + A\overline{B}\overline{D} + \overline{A}\overline{C}D + \overline{A}CD$, in order to simplify it using the Karnaugh mapping procedure, we first have to express it in canonical form, i.e.,

$$X = \overline{A}BC\overline{D} + \overline{A}\overline{B}C\overline{D} + \overline{A}B\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D} + A\overline{B}C\overline{D} + A\overline{B}\overline{C}\overline{D} + \overline{A}B\overline{C}D + \overline{A}\overline{B}\overline{C}D + \overline{A}BCD + \overline{A}\overline{B}CD$$

[2 Marks]

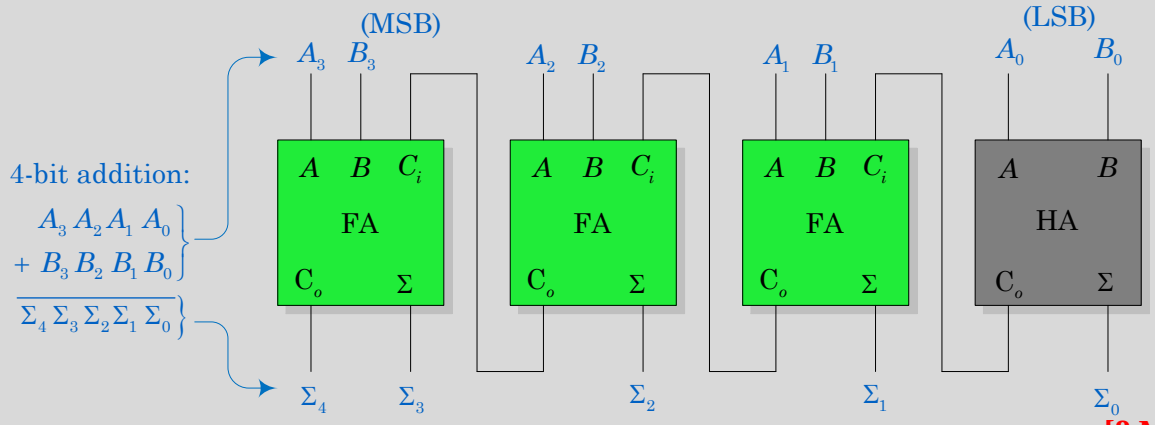
It follows from the canonical form the given expression that the Karnaugh map is as shown, with the appropriate groups.



[5 Marks]

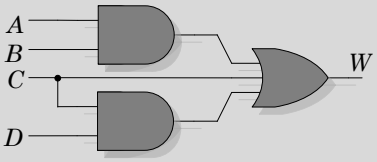
Therefore, the simplified expression is $X = \overline{A} + \overline{B}\overline{D}$.

(b) The 4-bit binary adder is as shown below.



[8 Marks]

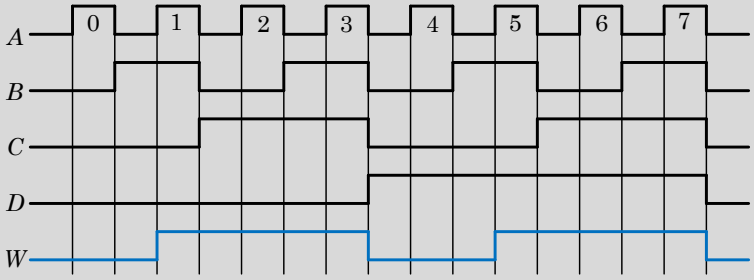
(c) The Boolean expression for the given logic circuit can be quickly found by following through the logic circuit from input to output taking not of the variable combinations to form terms.



Thus we get; $W = AB + C + CD$.

[1 Marks]

Therefore, the complete timing diagram is;



[4 Marks]

[Total 20 Marks]

END OF EEE 3131 EXAM MODEL SOLUTIONS