

THE UNIVERSITY OF ZAMBIA

SCHOOL OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

UNIVERSITY EXAMINATIONS

MID YEAR EXAMS – 2015/2016 – May 2016

EEE 3131

DIGITAL ELECTRONICS

TIME	: Three (3) hours
INSTRUCTIONS	: Answer any five (5) questions

QUESTION 1

a) For the following list of TTL ICs, describe their key features in terms of speed and power consumption as designated by their name.

- i. 7400 [2 Marks]
- ii. 74H00 [3 Marks]
- iii. 74L00 [3 Marks]
- iv. 74S00 [3 Marks]

b) A set of identical standard TTL NAND gates have the following current sourcing and sinking parameters: $I_{OH} = 400\mu A$, $I_{IH} = 80\mu A$, $I_{OL} = 16mA$ and $I_{IL} = 1.6mA$. The same set of NAND gates also has guaranteed voltage output of 0V to 0.4V for logic low and 2.4V to 5.0V for logic high. On the inputs, each gate has recognizable logic voltage range from 0V to 0.8V for logic low and 2.0V to 5.0V for logic high. If this type of NAND gate is used as a building block for a bigger digital circuit, i.e. interconnecting a number of the same NAND gates,

- i. Calculate the fan out and explain its significance. [4 Marks]
- ii. What is the maximum allowable magnitude of external stray voltage that can interfere with the circuit without causing undesirable performance of the digital circuit above? [5 Marks]

[Total 20 Marks]

QUESTION 2

a) Consider EPROM and EEPROM:

- i) What does each of the above acronyms stand for? [2 Marks]
- ii) What are the two main differences between the two? [2 Marks]
- iii) What is the major advantage of EEPROM over EPROM? [2 Marks]

b) Draw a NAND SR latch (with only two logic gates) and its associated truth table. [3 Marks]

c) State one limitation in the operation of the NAND SR latch in b) above and indicate how you would improve it by converting it to a level-triggered D-flip-flop (include logic circuit and clock signal). [5 Marks]

- d) For the JK flip-flop shown in Figure Q2(d) below, use the indicated clock signal to draw the timing diagram of the circuit when $J = K = 1$. Ensure that the timing diagram has four signals in the following order: the clock signal (sixteen clock pulses), J, K and the output signal (Q).

[4 Marks]

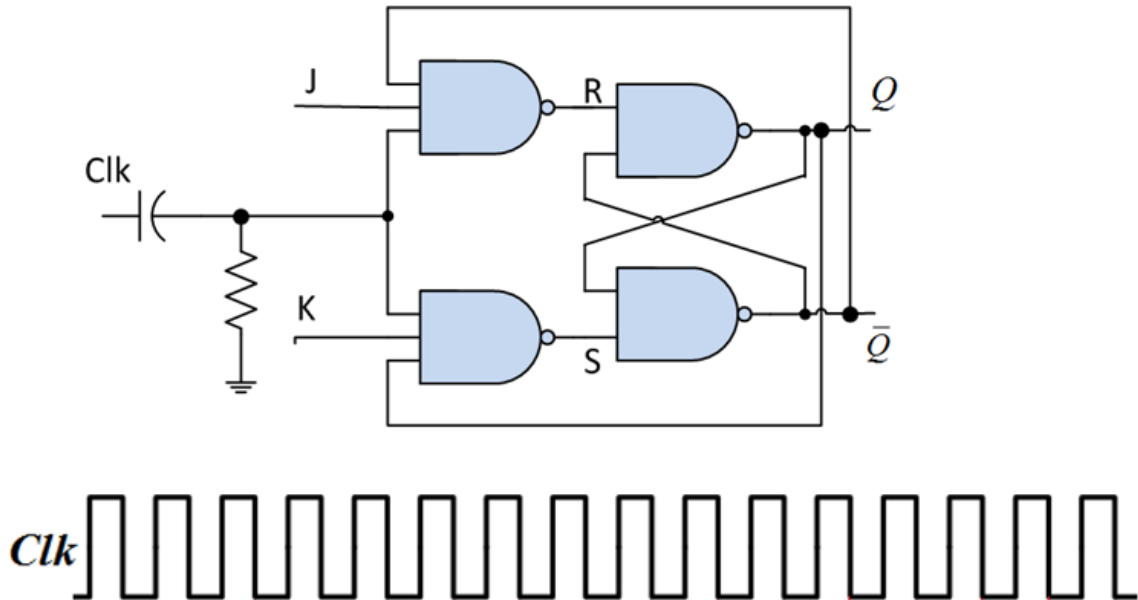


Figure Q2(d)

- e) State one of important advantage of a JK Master-Slave flip-flop over the ordinary JK flip-flop.

[2 Marks]

[Total 20 Marks]

QUESTION 3

- a)
- What is the main difference between a microprocessor and a microcontroller?
[2 Marks]
 - List two examples of microcontrollers commonly used in electronics.
[2 Marks]
- b) A simple 4-bit buffer register is shown in Figure Q3. Design a mechanism at its inputs that will turn it into a controlled buffer register where a LOAD signal can be used to load data when required or merely refresh the current contents when no new data is being loaded. Include a brief description of how the loading and the refreshing work.

[10 Marks]

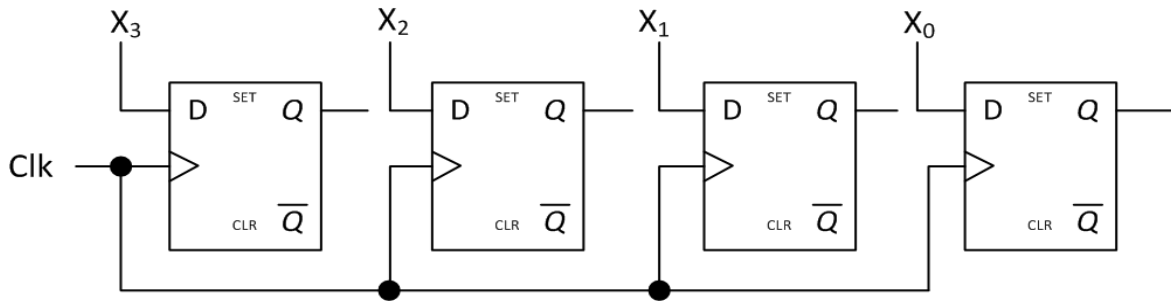


Figure Q3

- c) For the diode ROM in Figure Q3(c) below, design a solid-state alternative of addressing/accessing the memory locations as a replacement for the 5V mechanical rotary switch that is used to select a memory location. As a result, draw your designed addressing method (using logic gates) together with the diode ROM and its indicated contents. [6 Marks]

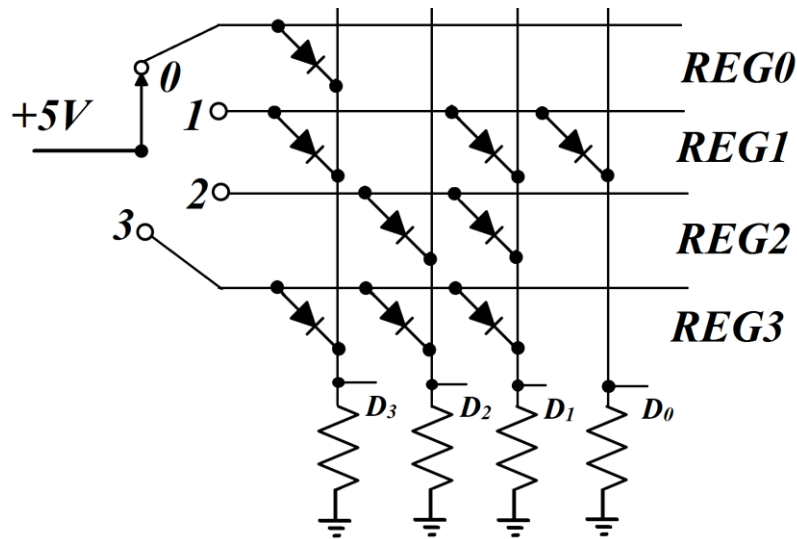


Figure Q3(c)

[Total 20 Marks]

QUESTION 4

- a)
- What is the minimum number of flip-flops required to make a MOD-32 binary counter? [2 Marks]
 - What is the terminal count, in decimal, of a synchronous ripple counter that uses five (5) flip-flops? [1 Marks]
 - A MOD-16 synchronous ripple counter has its current value at 1000_2 . What value will the counter have after 20 clock pulses? [2 Marks]
- b) For the controlled synchronous counter shown in Figure Q4(b) below, draw the timing diagram for sixteen (16) clock cycles. Your timing diagram should include, the counting

control signal (COUNT), the clock pulses (clk) and the contents of the flip-flops FF0, FF1, FF2 and FF3 in that order. [10 Marks]

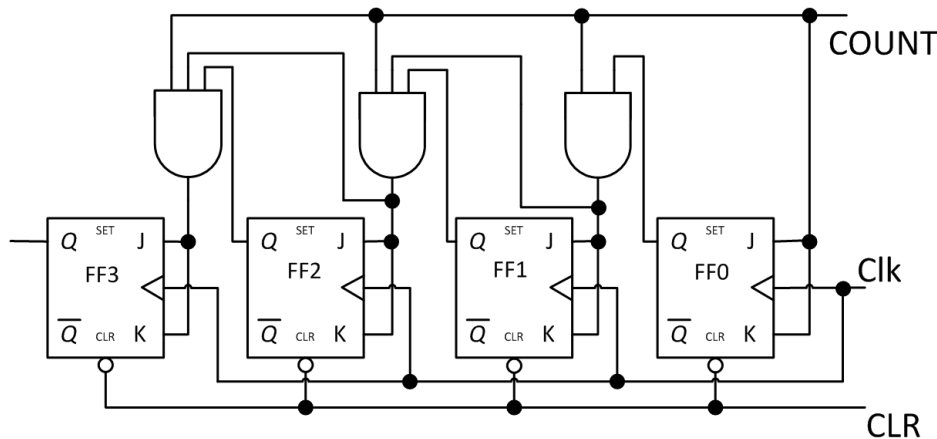


Figure Q4(b)

- c)
- i) List the three kinds of buses found in microprocessor based computer systems and state their functions. [3 Marks]
 - ii) What is the maximum number of memory locations that can be addressed on a computer system that uses a 16-bit address bus? [2 Marks]

[Total 20 Marks]

QUESTION 5

- a) A chemical plant needs a microprocessor-driven alarm system to warn of critical conditions in one of its chemical tanks. The tank has four HIGH/LOW (1/0) switches that monitor temperature (T), pressure (P), fluid level (L), and weight (W). Use the Karnaugh mapping procedure to design a system, that will notify the microprocessor to activate an alarm when any of the following conditions arise: [8 Marks]

1. High fluid level with high temperature and high pressure
2. Low fluid level with high temperature and high weight
3. Low fluid level with low temperature and high pressure
4. Low fluid level with low weight and high temperature

- b) The sum of products Boolean expression in short form notation is given by $f(A, B, C, D) = \sum 0, 1, 2, 3, 9, 11, 12, 14 + \sum_d 8, 10$, where the second summation over d

denotes the 'don't care' conditions.

- i) Draw the Minterm Karnaugh map for the given expression. [8 Marks]
- ii) Using the Karnaugh map in i) find the minimized Boolean expression. [2 Marks]
- iii) Hence, draw the minimized logic circuit. [2 Marks]

[Total 20 Marks]

QUESTION 6

- a) Convert the hexadecimal number ABFH to its Gray code equivalent. [3 Marks]
- b) Subtraction in binary can be performed by addition of signed 2's complement of operands.
 - i) Using signed 2's complement notation, express as 8 bit words the decimal numbers +42 and -23. [3 Marks]

ii) Hence, perform in 2's complement notation the arithmetic operation $+42 - 23$. **[2 Marks]**

c) Design a two's complement binary adder/subtractor circuit which adds two 8-bit binary words based on two **4008-CMOS** adders (ICs). Hence, prove that the subtraction $+42 - 23$ produces the correct answer at the outputs by labeling the input and output lines on your circuit design. **[12 Marks]**

[Total 20 Marks]

QUESTION 7

a) Simplify the following Boolean expression using the Karnaugh mapping procedure.

$$X = \overline{A}\overline{D} + \overline{A}B\overline{D} + \overline{A}C\overline{D} + \overline{A}CD \quad \text{[7 Marks]}$$

b) Design a 4-bit binary adder based on Full-Adder and Half-Adder block diagrams. **[8 Marks]**

c) Consider the circuit and input timing diagrams in Figure Q7. Write the Boolean expression and complete the timing diagram at W . **[5 Marks]**

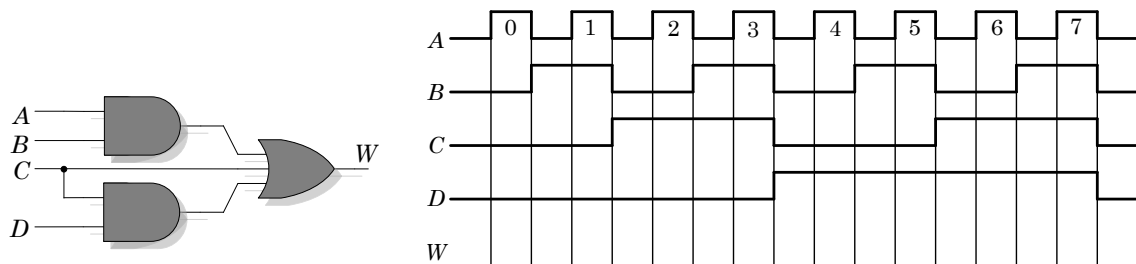


Figure Q7.

[Total 20 Marks]

Wish You Success!

END OF EEE 3131 EXAMINATION