THE UNIVERSITY OF ZAMBIA

SCHOOL OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

LAB 2 REPORT

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COURSE: EEE 3131

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1.0 TITLE:

THE SIMPLE LATCH AND CLOCKED FLIP-FLOPS

2.0 OBJECTIVES

- Understanding the importance of feedback and appreciate its role in memory storage.
- To examine the basic unclocked and clocked flip-flops (bistables or memories); the latch, the clocked RS and the clocked D types.

3.0 THEORY

There are various ways of connecting logic gates in order to get an intended output. Several different types of Integrated Circuit Logics are available.

Integrated Circuit Logic NAND is the easiest and cheapest operation to achieve and is therefore more widely used in practice as a logic element than any other.

This is why even in Sequential logic circuits discussed in this experiment, the two used logic gates are NAND and NOT for all the intended outputs.

The simple latch circuit responds to changes in its input as soon as they occurred - a circuit like this is often called 'àsynchronous' because its behaviour is not synchronised with any timing signals.

Another circuit we shall study is arranged so that changes to its inputs take effect only when a brief clock-pulse or timing signal is applied. This is achieved by the addition of two NAND gates to the circuit so as to control the input signals by a common clock signal. These inputs are now called SET (S) and RESET (R) whilst the outputs are labelled Q and Q' on the assumption that they will always be complementary (that is simultaneous '0' inputs to both sides of the latch will not be allowed).

4.0 EQUIPMENT REQUIRED

- Multisim software
- Hp ENVY laptop

5.0 PROCEDURE

Practical 5.1: FEEDBACK LOOP

Set up the circuit as instructed in the lab manual and simulate on multism software

Practical 5.2: SR LATCH

Set up the circuit as instructed in the lab manual and simulate on multism software

Practical 5.3: **CLOCKED SET-RESET FLIP-FLOP**

Set up the circuit as instructed in the lab manual and simulate on multism software

Practical 5.4: D FLIP-FLOP

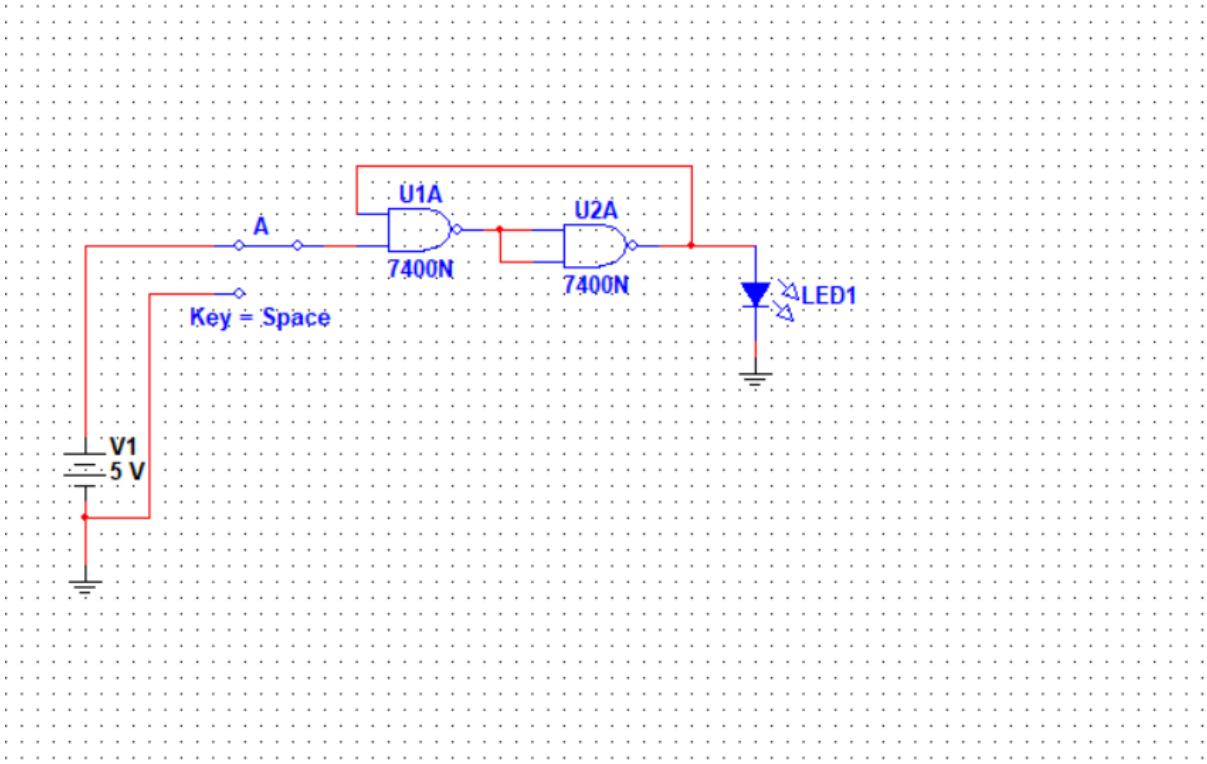
Set up the circuit as instructed in the lab manual and simulate on multism software

Practical 5.5: EDGE TRIGGERED D FLIP-FLOP

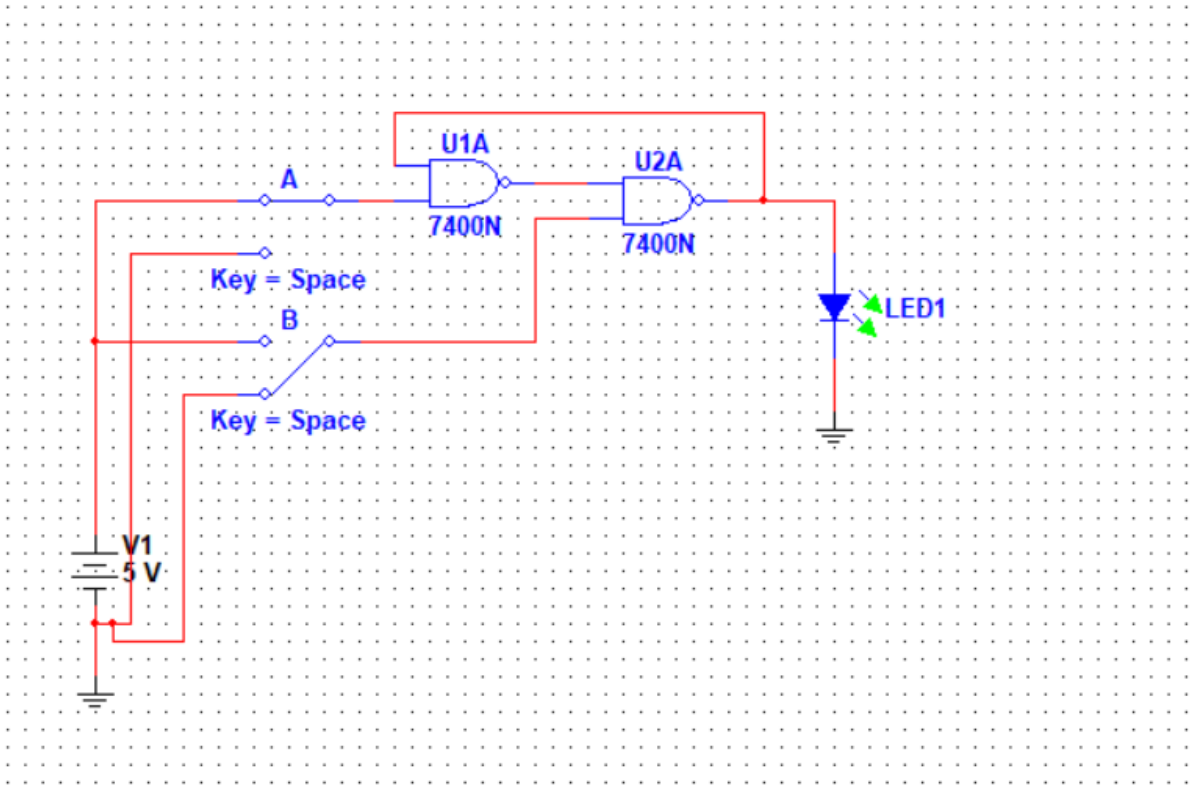
Set up the circuit as instructed in the lab manual and simulate on multism software

6.0 RESULTS

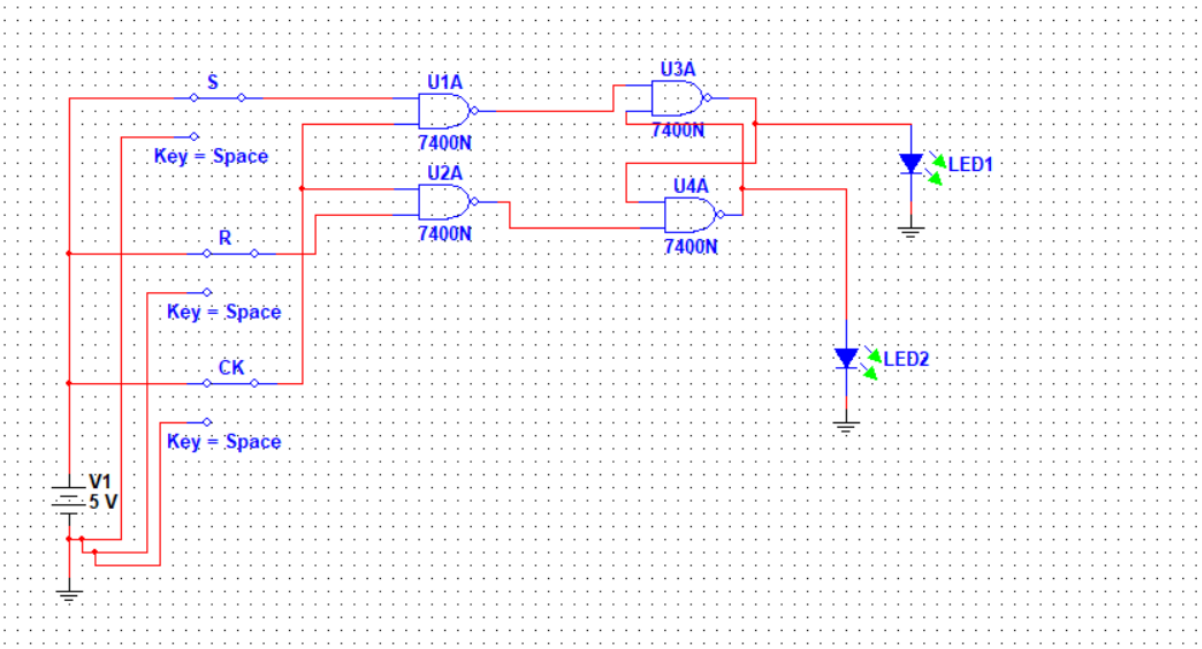
PRACTICAL 5.1



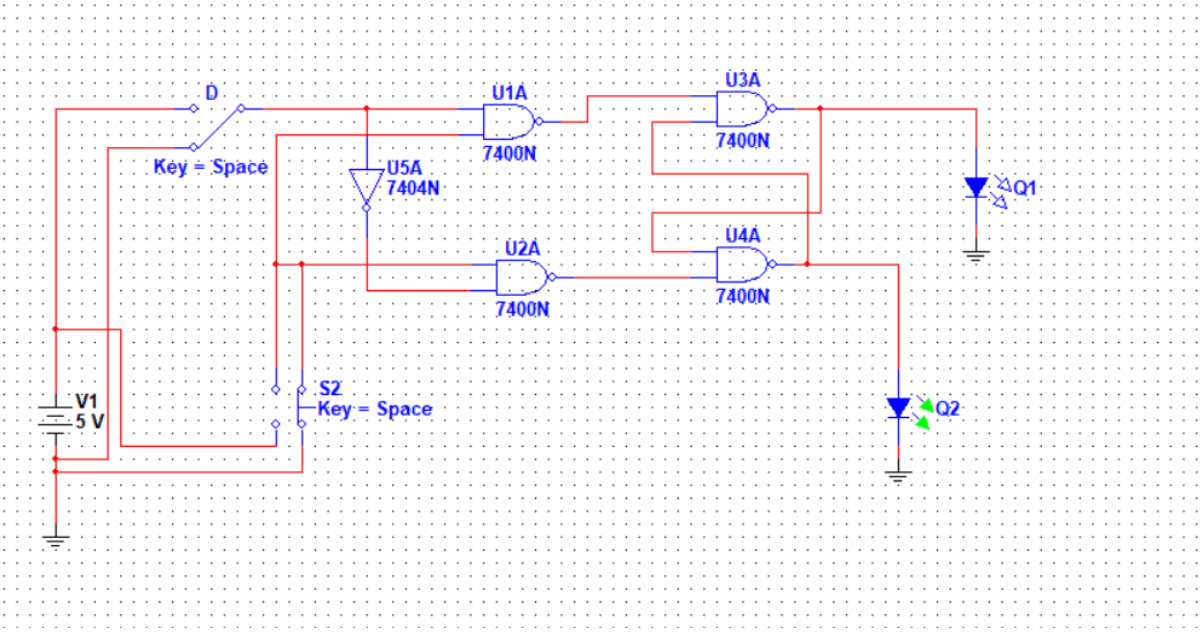
PRACTICAL 5.2



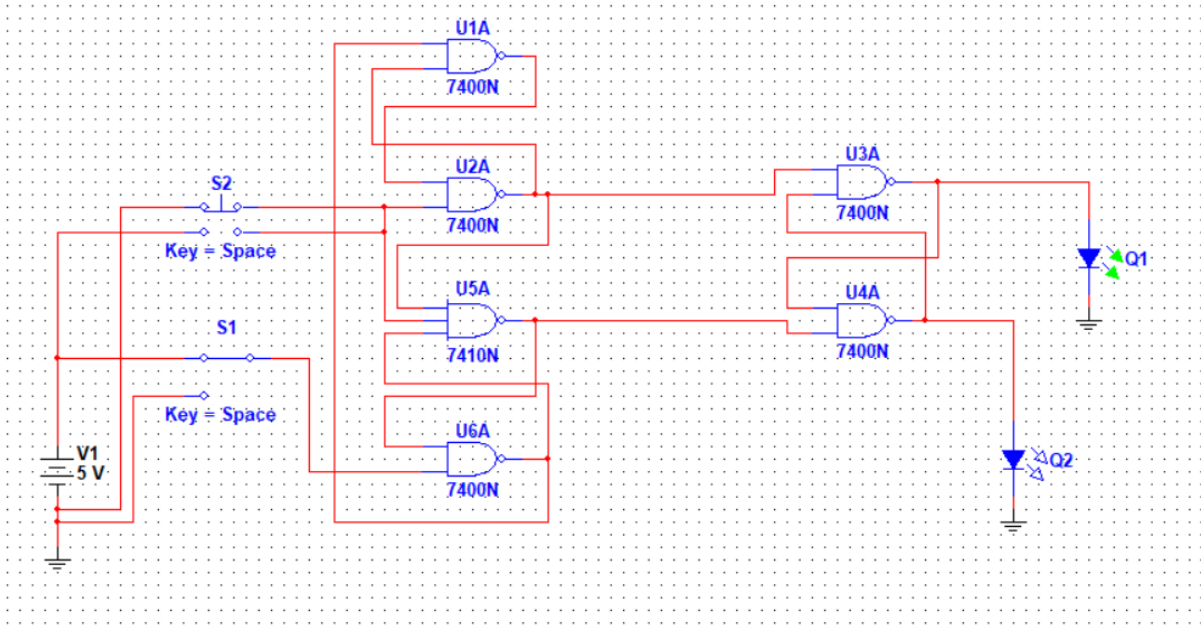
PRACTICAL 5.3



PRACTICAL 5.4



PRACTICAL 5.5



7.0 DISCUSSION.

In this experiment, we consider circuits whose outputs are determined partially or entirely by inputs that occurred in the past. In other words circuits having a memory. These are called 'sequential logic' networks.

Sequential networks have outputs determined to some extent by past inputs. Their outputs remain constant until a specific combination of the inputs is altered. This is because of the implementation of positive feedback loop. The output is unaffected when neither of the inputs is set to TRUE. But when one of the inputs is set to true the output will always produce a specific output.
The Clocked Set-Reset Flip-Flop is arranged so that changes to its inputs take effect only when a brief clock-pulse or timing signal is applied. This is achieved by the addition of two NAND gates so as to control the input signals by a common clock signal.

The outputs of the circuits were indicated by an LED, which lit up when the output was '1' or in other terms 5V (HIGH) and was off when the output was '0' or in other terms 0V (LOW)

For instance 1 and 0 can represent any of the pairs of opposites shown in the following table.

1	'0'
TRUE	FALSE
IN	OUT
YES	NO

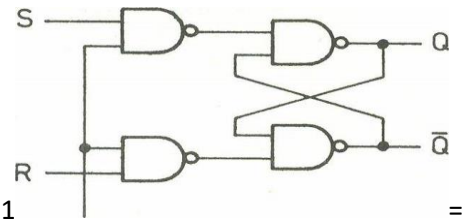
8.0 ANSWERS TO EXERCISES

EXERCISE 5.1

S	**R**	**Q_{n+1}**
0	**0**	**Q_n**
0	**1**	**0**
1	**0**	**1**
1	**1**	**INVALID**

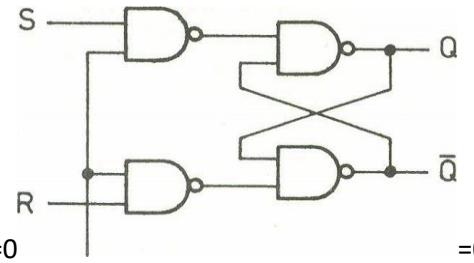
EXERCISE 5.2

=0 =0



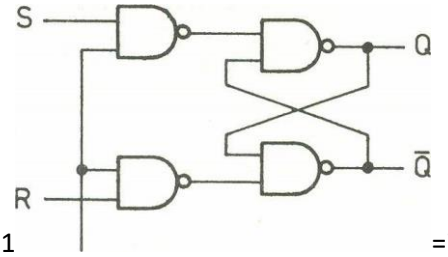
=1 =1

=1 =1



=0 =0

=1 =?



=1 =?

EXERCISE 5.3

Clock	0	1	2	3	4	Q	Q’
0	0	-	-	-	-	-	-
0	1	-	-	-	-	-	-
1	0	0	1	0	1	0	1
1	1	1	0	1	0	1	0

9.0 CONCLUSION

The experiment was successfully done as the objectives were met. All connected circuits, when simulated in multism, responded in accordance with their respective truth tables.

The effect of the FEEDBACK loop was observed and the Clocked Set-Reset Flip-Flop was better understood by observing, studying and analysing how the output changed with various connections.

10.0 APPLICATIONS

The simple unclocked latch and the clocked SR forms are often enough used in constructed circuits, just as was done in the experimental procedures above.

But it is worth noting that they are not usually in cooperated in the families of commercial integrated circuits. This is because the unclocked latch is easily constructed from two NAND gates and thus not worth making in integrated form.
Another reason is that the clocked SR form is restricted in its use by the uncertainty which arises when S and R are both '1'.

This uncertainty can be resolved by the addition of further logic as shall be further explained at a later stage.

11.0 REFERENCES

[1] William Kleitz, 2006, Digital Electronics with VHDL, Prentice Hall ISBN-100131714902 [Practical 1]

[2] Maini Anil K., Digital Electronics: Principles, Devices and Applications, 2007, John Wiley and Sons Ltd, ISBN 978-0-470-03214-5. [Theory 1]

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[4] Sedha R.S, A textbook of Digital Electronics, S. Chand, 2010 [Theory 2]

[5] Alan C. Diixon, JamesL. Antonakos, 2000, A Practical Approach To Digital Electronics, Prentice Hall ISBN-10: 0137275 951.