THE UNIVERSITY OF ZAMBIA

SCHOOL OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

ASSIGNMENT 5 SOLUTIONS

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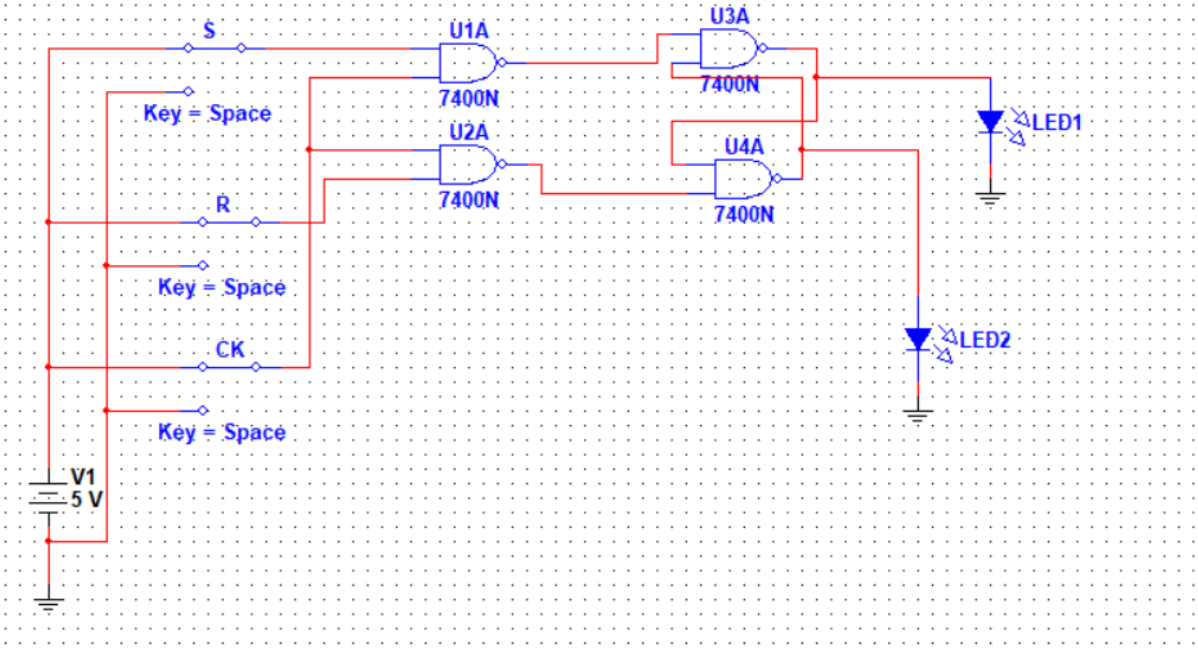
COURSE: EEE 3131

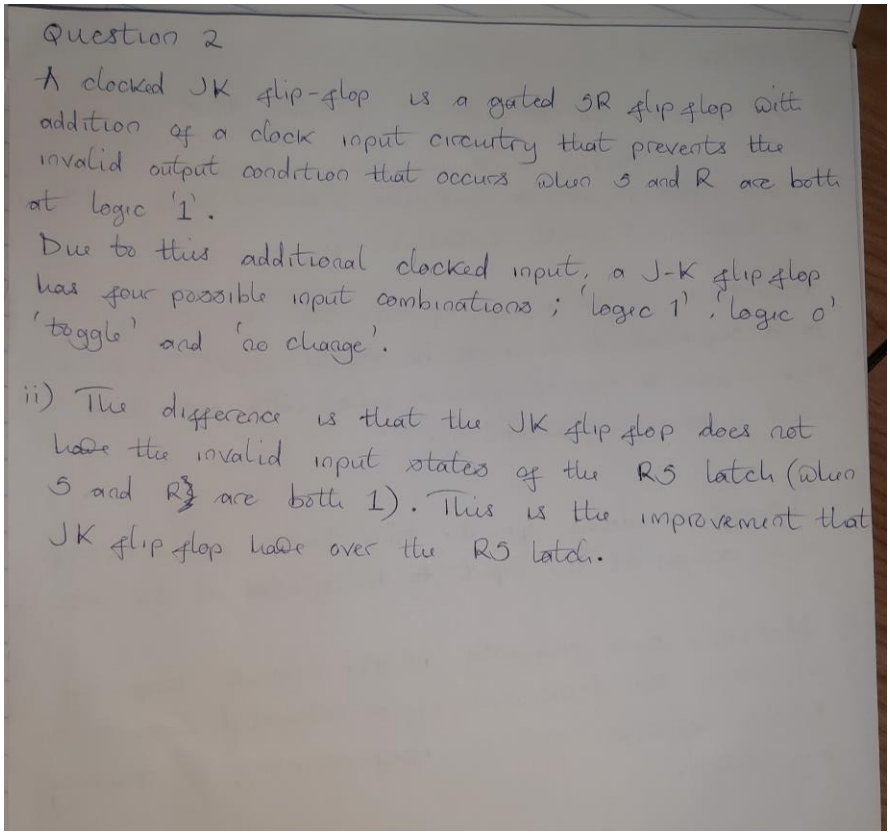
LECTURER: MR GEORGE ZIBA

Question 1



Clock	R	S	Q
1	0	0	Qn
1	0	1	1
1	1	0	0
1	1	1	invalid

Question 2



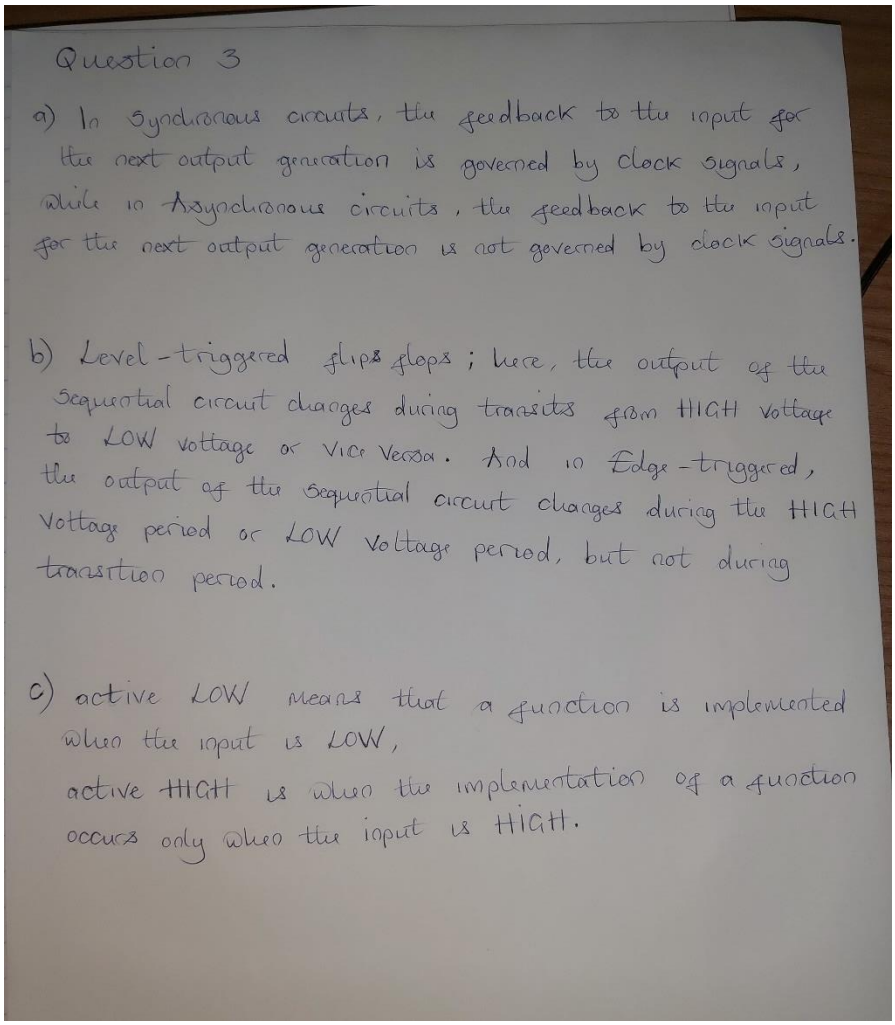
Question 2

A clocked JK flip-flop is a gated SR flip flop with addition of a clock input circuitry that prevents the invalid output condition that occurs when S and R are both at logic '1'.

Due to this additional clocked input, a J-K flip flop has four possible input combinations; 'logic 1', 'logic 0' 'toggle' and 'no change'.

ii) The difference is that the JK flip flop does not have the invalid input states of the RS latch (when S and R are both 1). This is the improvement that JK flip flop have over the RS latch.

Question 3



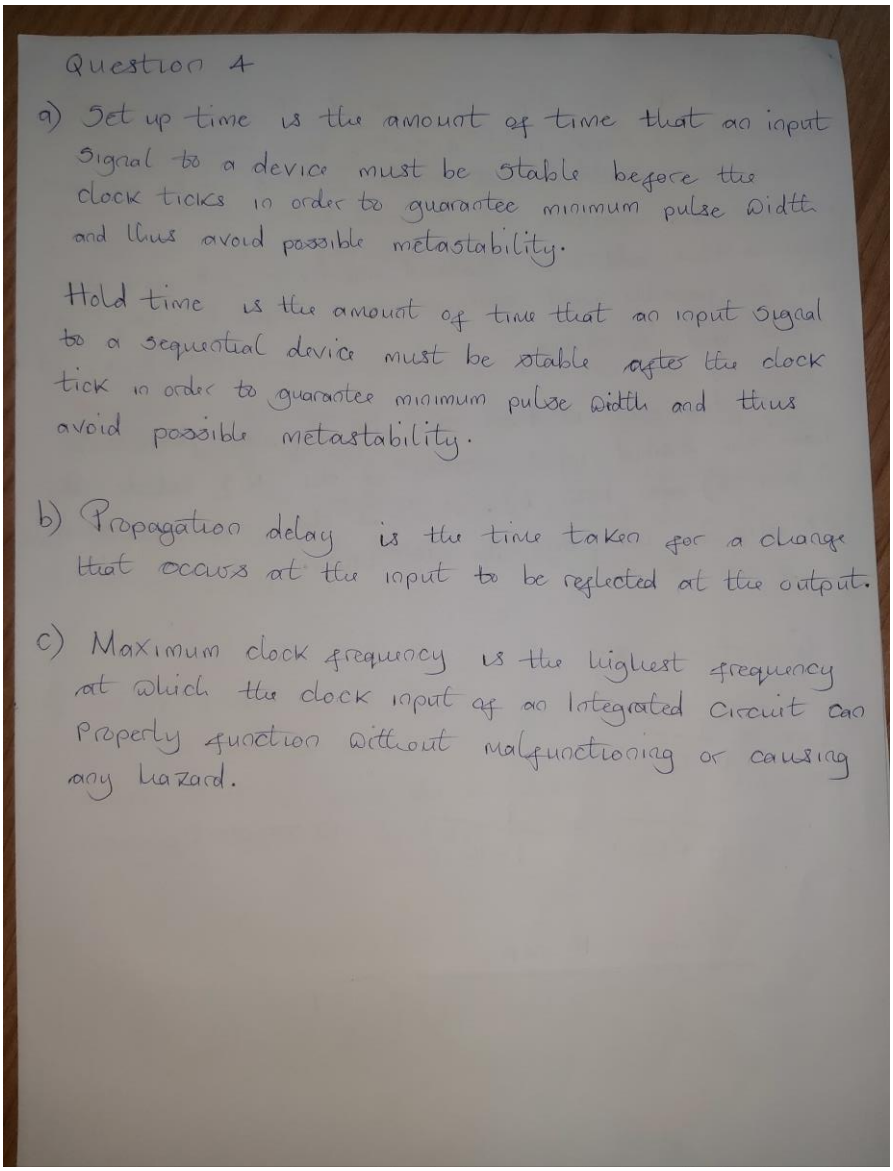
Question 3

a) In synchronous circuits, the feedback to the input for the next output generation is governed by clock signals, while in Asynchronous circuits, the feedback to the input for the next output generation is not governed by clock signals.

b) Level-triggered flips flops ; here, the output of the sequential circuit changes during transits from HIGH voltage to LOW voltage or vice versa. And in Edge-triggered, the output of the sequential circuit changes during the HIGH voltage period or LOW voltage period, but not during transition period.

c) active LOW means that a function is implemented when the input is LOW,
active HIGH is when the implementation of a function occurs only when the input is HIGH.

Question 4



Question 4

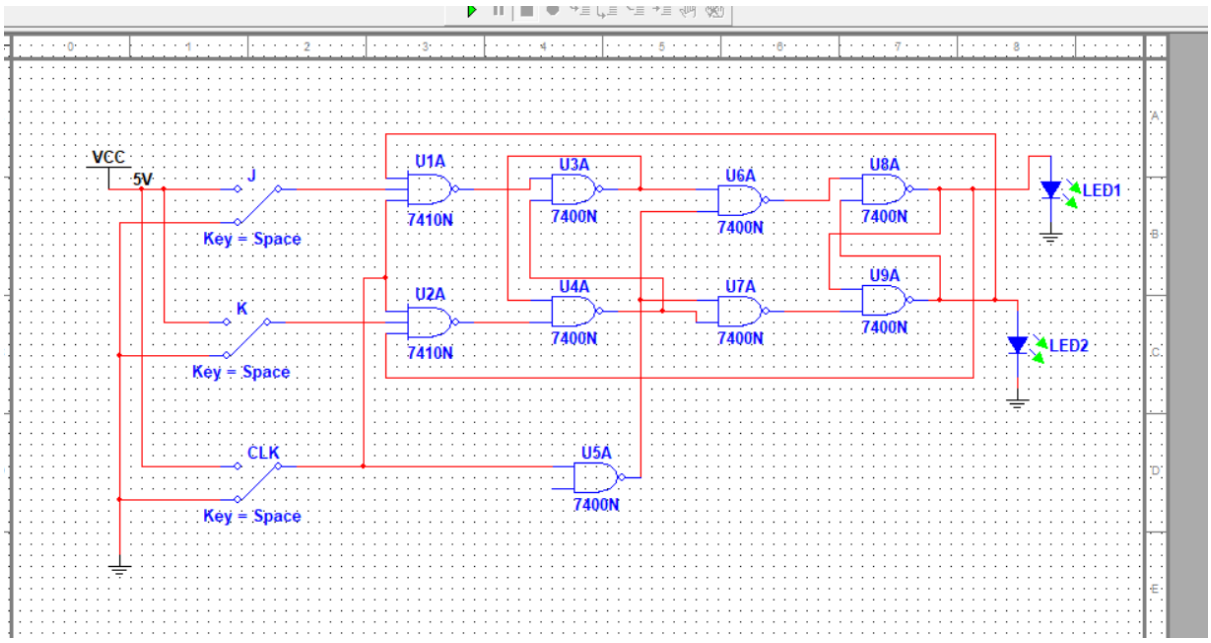
a) Set up time is the amount of time that an input signal to a device must be stable before the clock ticks in order to guarantee minimum pulse width and thus avoid possible metastability.

Hold time is the amount of time that an input signal to a sequential device must be stable after the clock tick in order to guarantee minimum pulse width and thus avoid possible metastability.

b) Propagation delay is the time taken for a change that occurs at the input to be reflected at the output.

c) Maximum clock frequency is the highest frequency at which the clock input of an integrated circuit can properly function without malfunctioning or causing any hazard.

Question 5



j	k	Qn	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Qn \ JK

	00	01	11	10
0	0	0	1	1
1	1	0	0	1

$Q_{n+1} = J'.Q_n + K'.Q_n$

Question 6

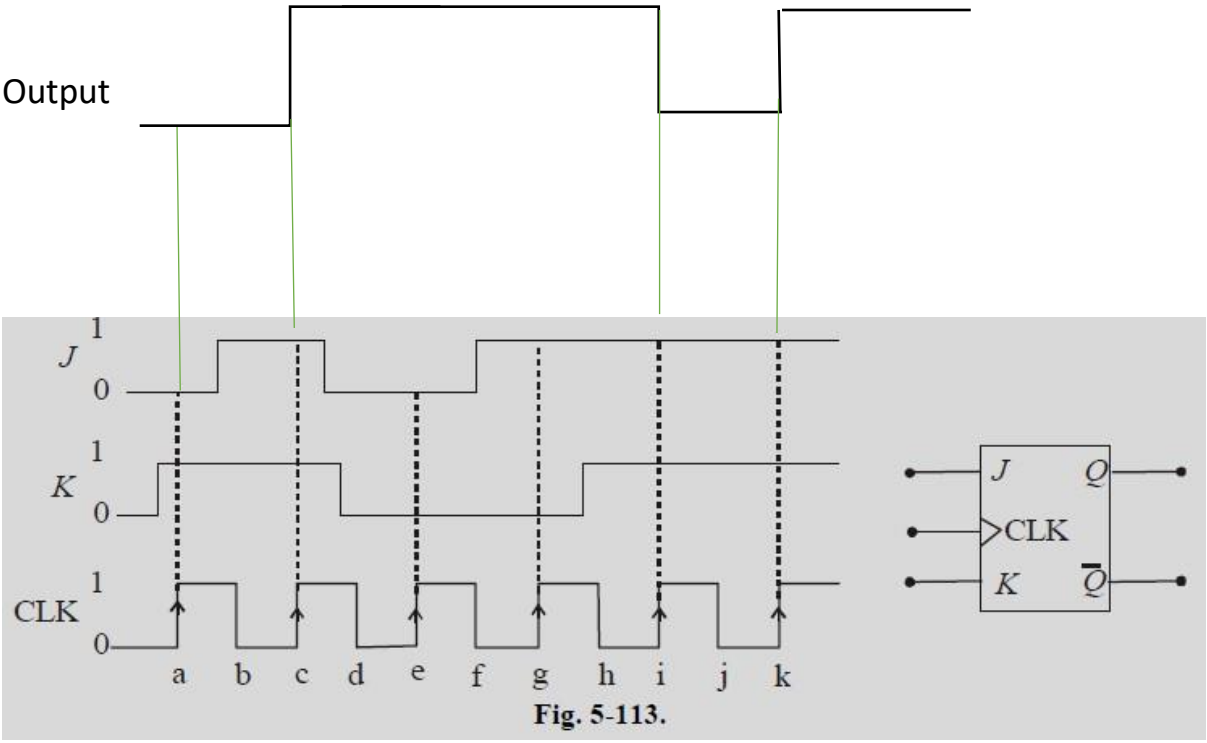
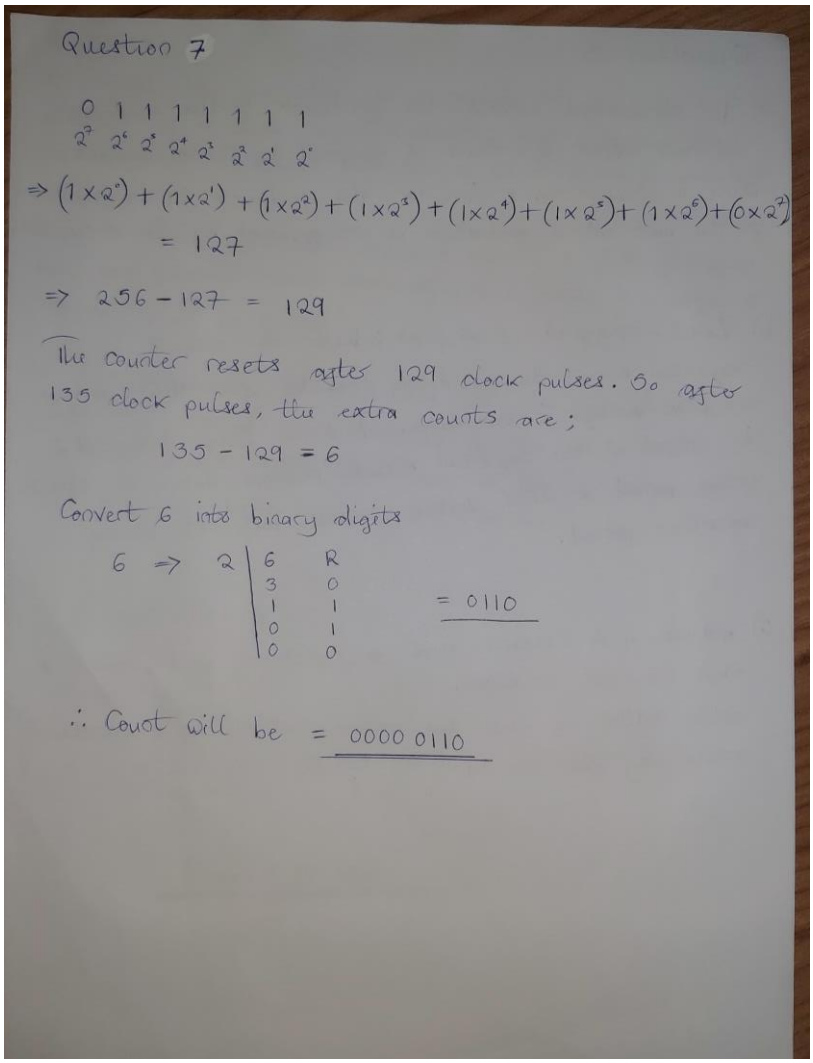
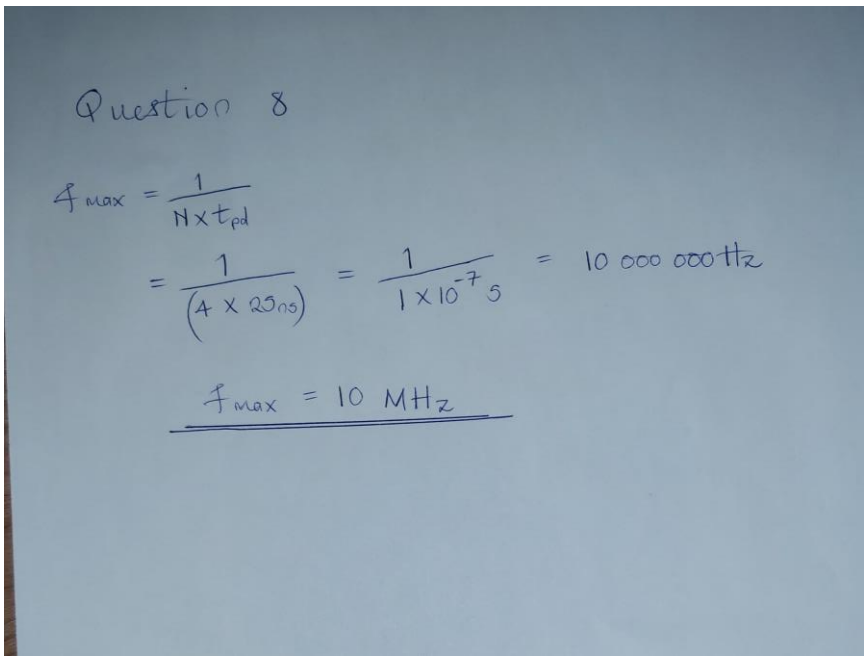


Fig. 5-113.

Question 7


Question 7
0 1 1 1 1 1 1 1
2^7 2^6 2^5 2^4 2^3 2^2 2^1 2^0
$\Rightarrow (1\times2^0)+(1\times2^1)+(1\times2^2)+(1\times2^3)+(1\times2^4)+(1\times2^5)+(1\times2^6)+(0\times2^7)$
$= 127$
$\Rightarrow 256 - 127 = 129$
The counter resets after 129 clock pulses. So after 135 clock pulses, the extra counts are;
$135 - 129 = 6$
Convert 6 into binary digits
$6 \Rightarrow 2$ | 6 R | 3 0 | 1 1 | 0 1 | 0 0
$= 0110$
$\therefore$ Count will be $= 0000\ 0110$

Question 8


Question 8
$f_{max} = \frac{1}{N \times t_{pd}}$
$= \frac{1}{(4 \times 25ns)} = \frac{1}{1 \times 10^{-7} s} = 10\,000\,000 Hz$
$f_{max} = 10\ MHz$