THE UNIVERSITY OF ZAMBIA

SCHOOL OF ENGINEERING

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

ASSIGNMENT 3 SOLUTIONS

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COURSE: EEE 3131

ATTENTION: MR GEORGE ZIBA

Question 1

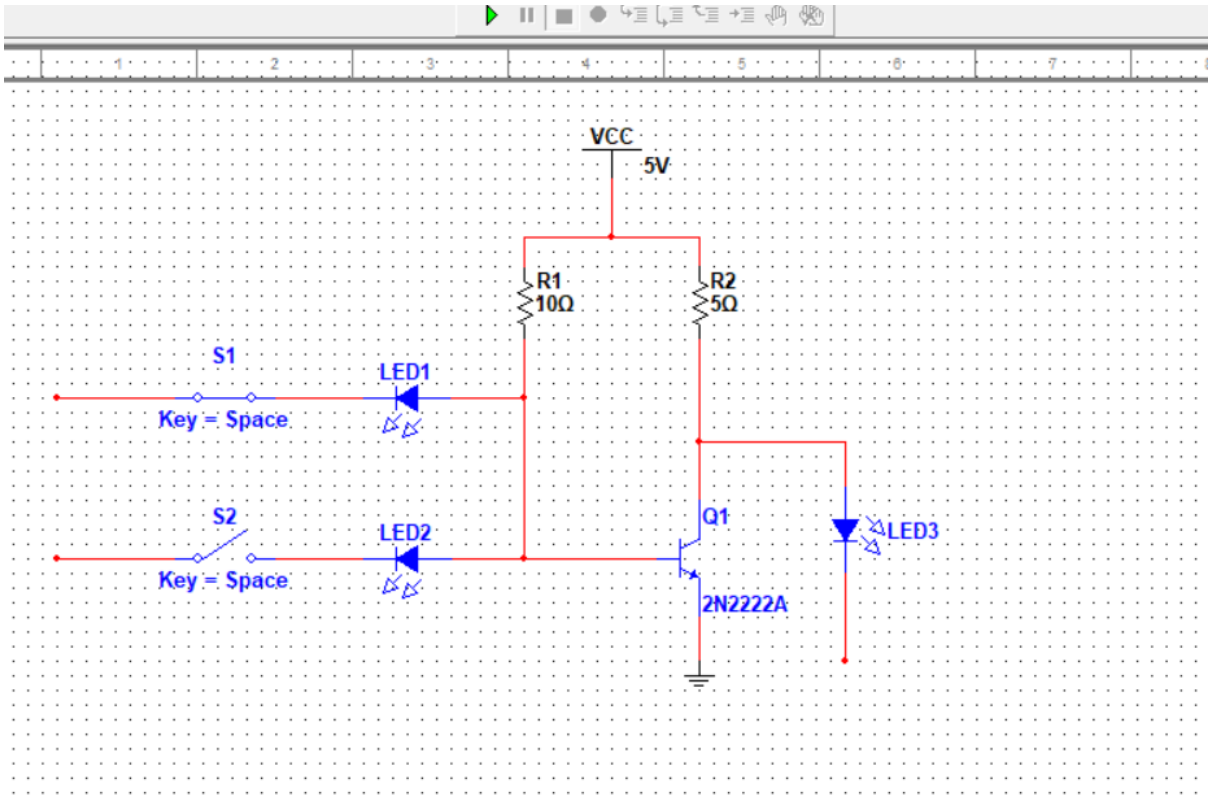
a) - In an IC, the various components are part of a small semiconductor chip and these individual components cannot be removed or replaced in case of damage. So, instead, the entire IC would have to be replaced in case of damage.

- ICs cannot withstand rough handling or excessive heat, so they require quite delicate handling.

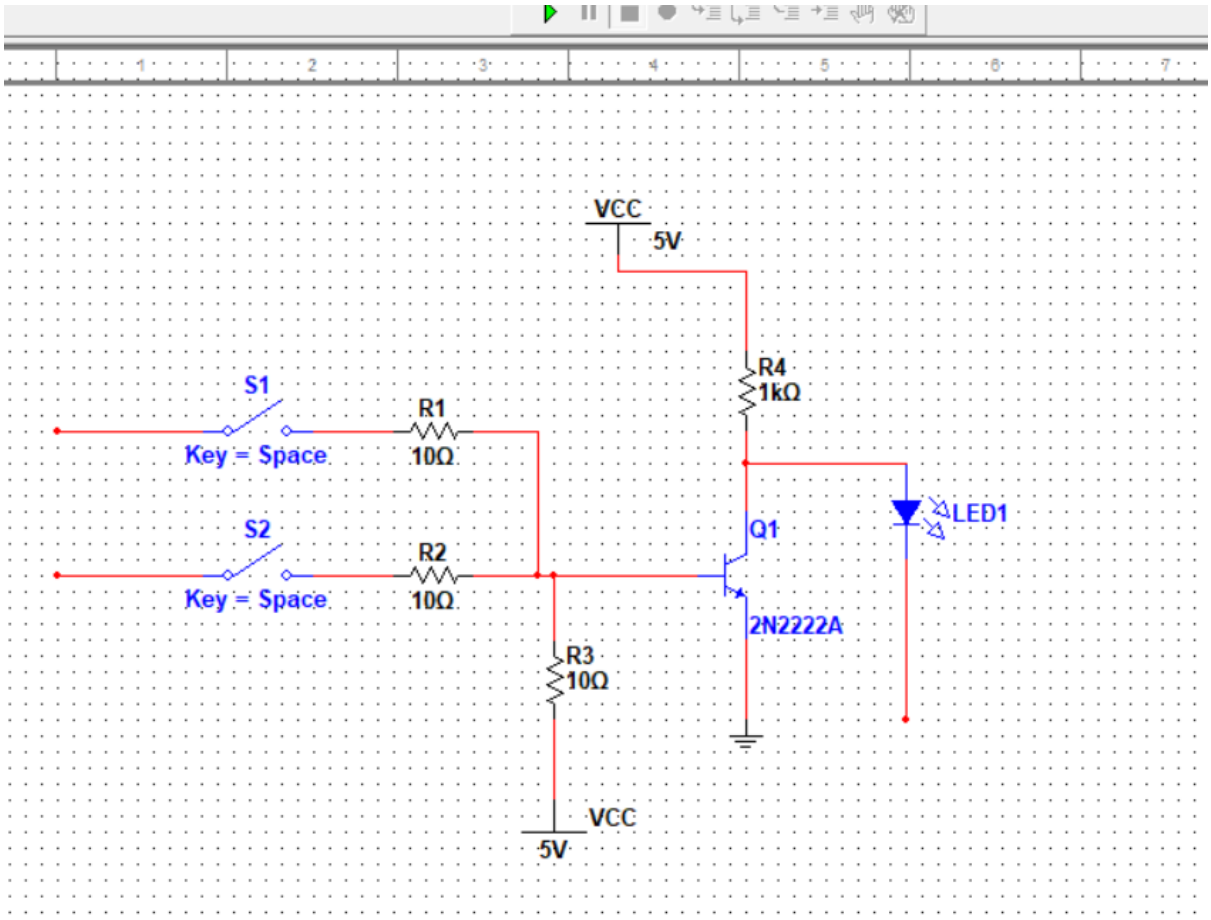
b) Fanout = $\frac{I_{OH}}{I_{IH}}$ $\qquad$ $\frac{I_{OL}}{I_{IL}}$

$= \frac{1.0mA}{0.02mA} = 50$ $\qquad$ $= \frac{20.0mA}{0.4mA} = 50$

Q2a.


VCC
5V
R1
10Ω
R2
5Ω
S1
LED1
Key = Space
S2
LED2
Key = Space
Q1
LED3
2N2222A

Q2b.


VCC
5V
R4
1kΩ
S1
Key = Space
R1
10Ω
LED1
Q1
S2
Key = Space
R2
10Ω
2N2222A
R3
10Ω
VCC
5V

Question 2

a) When both switches (inputs) are at 0V, the two diodes are both in ON condition.

Through LED 1 and LED 2, the supply voltage will find paths to the ground.

Now, the supply voltage will drop across the resistor, leaving the transistor in the OFF state. Hence, the supply voltage will be reflected at the LED 3, which is the output, making it to be in the ON state.

- In the case where both inputs are at 5V, both the diodes, LED 1 and LED 2 will be in the OFF state. In consequence, the transistor will be in the ON state and this supply voltage will find a path to the ground.

The output, LED 3 gets no voltage, leaving it at Zero, (0) logic level.

Therefore, the output is 1 only when both inputs are 0 (0V).

2b) RTL fall under Bipolar Junction Transistors.

A bipolar transistor switch is the simplest RTL gate (Resistor-Transistor Logic). The base resistor is connected between the base and input voltage source.

This base resistor has the role of expanding the very small transistor input voltage range to the logic level '1' by converting the input voltage into current. The value has to be low enough to saturate the transistor and high enough to obtain high input resistance.

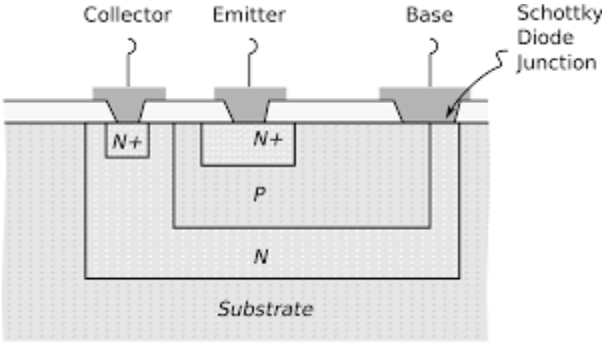
The collector resistor is used to convert the collector current into voltage. The resistance should be high enough to saturate the ~~resistor~~ transistor and low enough to obtain low output resistance.

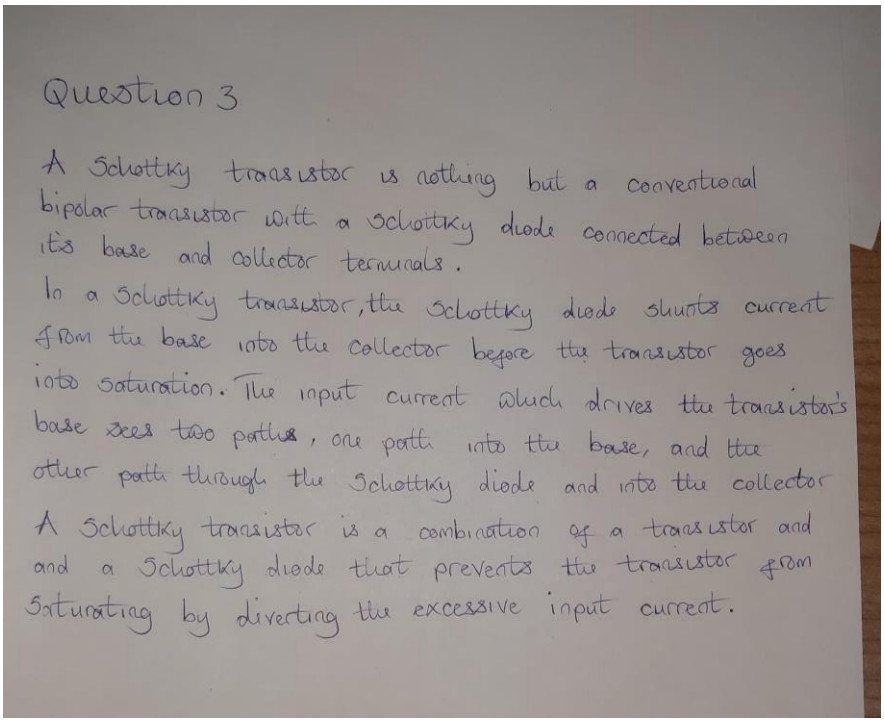
When two or more base resistors are used, the inverter becomes a two input RTL NOR gate.

The ~~resis~~ base resistances and the number of inputs are chosen so that only logic level '1' is sufficient to create base-emitter voltage exceeding threshold and in turn, saturating the transistor.

Limitations of one transistor RTL NOR gate are overcome by the multi-transistor RTL implementation. This consists of a set of parallel-connected transistor switches driven by logic inputs. In this configuration, the inputs are completely separated and the number of inputs is limited only by the small leakage current of the cut-off transistors at output logical level '1'.

Question 3





Question 3

A Schottky transistor is nothing but a conventional bipolar transistor with a Schottky diode connected between its base and collector terminals.

In a Schottky transistor, the Schottky diode shunts current from the base into the collector before the transistor goes into saturation. The input current which drives the transistor's base sees two paths, one path into the base, and the other path through the Schottky diode and into the collector

A Schottky transistor is a combination of a transistor and and a Schottky diode that prevents the transistor from saturating by diverting the excessive input current.

Question 4

Power dissipation is mostly defined in terms of power consumption, and in this case, we'll define it in terms of power consumption of logic families, TTL and CMOS.

- TTL chips consume more power compared to CMOS chips even at rest. ~~One of the major factors (which is clock rate) is~~
- One major factor for power consumption is the clock rate. Higher clock values will result in higer power consumption.

TTL have greater speed; with a lower propagation delay and higher power dissipation than CMOS.

Current requirements of the CMOS are low, and thus power consumption is limited.

The 'output' power of the CMOS is higher and it is smaller in size.

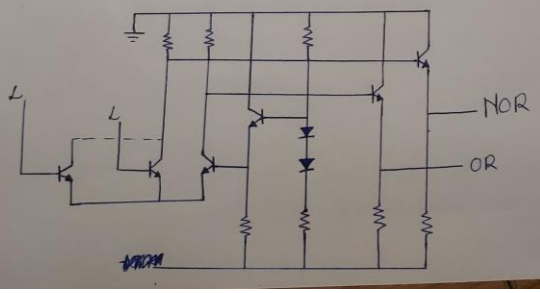
Question 5

The NOR/OR gate implemented using ECL is a high speed type of logic using transistors. If either one of the inputs is high, then the OR output is high, and the NOR output is low. If they are both low, then the OR output is low, but NOR output is high.

In the diagram depicted below, base voltage of Q3 is at a fixed level, with enough current to cause Q3 to conduct. This now causes the Q3 collector to go down, bringing the OR output low.

The Emitter of Q3 is high enough in relation to Q2's base. This ensures Q2 does not conduct, causing the Collector of Q2 to remain at ground level. This arrangement keeps the NOR output HIGH.

The corresponding transistor conducts if either of the inputs is HIGH. In this case, the NOR output is LOW, as the collectors of Q1 and Q2 are low.
The emmitters of Q1 and Q2 are HIGH enough to cause the Q3 to NOT conduct, making the OR output HIGH.



Question 6

a) Fan-out

b) High-level Input Current , I_{IH}
LOW-level Input Current , I_{IL}
HIGH-level output Current , I_{OH}
LOW-level output Current , I_{OL}

c) The presence of a Schottky diode does not allow the transistor to go to deep saturation.
A Schottky transistor is simply a ~~diode~~ bipolar transistor with a Schottky diode connected between its base and collector terminals.

Question 7

a) Negative number indicates that current is going into the output as opposed to out of the output.

b) Sink current is higher

c) TTL - Bipolar Junction transistor
CMOS - Field effect transistor

d) ECL has such high operating and switching speeds because it is a Non-saturating logic. The transistors are always operated in the active region and never driven to saturation or cut off.

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b) Fan out = $\frac{I_{OH}}{I_{IH}}$ $\frac{I_{OL}}{I_{IL}}$

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Question 8

a) The time of one cycle of V_{in} = 100μs + 120μs
= 220μs

$f = \frac{1}{t_p} = \frac{1}{220 \times 10^{-6}}$

$= \frac{1}{0.00022}$ Hz = 4545.4545

f of V_{in} = 4.55 kHz $\quad T = \frac{1}{f} = \frac{1}{4545.4545}$

T = 220 μs

b) t_r - the time length taken ~~from~~ for a pulse to rise from its 10% point to its 90% point.

$\therefore t_r = 2\mu s$

t_f - length of ~~the~~ time taken to fall from 90% to 10% point. Time taken to fall from 4.5V to 0.5V

$\therefore t_f = 3\mu s$

c) t_{PLH} - propagation delay for the output to respond to change from LOW-to-HIGH direction

$= t_{PLH} = 8\mu s = t_{PLH}$

$t_{PLH} = 8\mu s$

t_{PHL} - propagation delay for the output to respond to change from HIGH-to-LOW

$t_{PHL} = 6\mu s$

Question 9

The output of gate 3 is LOW (0), as its inputs ~~is~~ are 1 and 1.

Taking the typical value, $V_a = 0.2V$

Now since the output of gate 3 is LOW, there is a sink current drawn from the other three gates, namely, 4, 5 and 6.

Taking the typical value to each gate, $I_{IL} = 1.6mA$

So since these are three gates;

$I_a = 1.6mA \times 3 = 4.8mA$

$\therefore V_a = 0.2V \quad I_a = 4.8mA$

Question 10

Propagation delay - is the time delay or time taken for output to respond to the change in the logical level at the input.
-This change in the input logical level is either from HIGH-to-LOW, or from LOW-to-HIGH.

Power dissipation - is the product of supply voltage Vcc, and supply current Icc. for a particular logic family.
-It is defined mostly in terms of power consumption.

Speed-power product - The propagation delay of a logic circuit can be reduced, but this is at the expense of the power dissipation. It is very useful to have both Propagation delay and power dissipation as low values in a logic family, and this characteristic is a very useful figure-of-Merit to evaluate different logic families. This product is ~~measured~~ ~~in~~ expressed in picojoules.

Fan-out : Is the number of inputs of a logic function that can be driven from a single output without causing any false output. This is a characteristic of the logic family to which the device belongs, and can be computed from I_{OH}/I_{IH} in the logic HIGH and from I_{OL}/I_{IL} in the logic LOW state.

In the case where the two values are different the fan-out is taken as the smaller value.

Q10 cont.

Noise margin - of a gate is the maximum noise voltage that can be added to an input signal without causing undesirable outputs.

The undesirable output, which is the noise, is in form of DC, and it is caused by voltage level drift and also from AC noise caused by random pauses of other switching circuits etc.

Noise margin is calculated using voltage levels of the input signal and output signal.