Assignment five (5)

(1) What is a flip-flop? Show the logic implementation of an R-S flip-flop having active HIGH **R** and **S** inputs. Draw its truth table and mark the invalid entry.

(2) What is a clocked J-K flip-flop? What improvement does it have over a clocked R-S flip-flop?

(3) Differentiate between:

- (a) synchronous and asynchronous inputs;
- (b) level-triggered and edge-triggered flip-flops;
- (c) active LOW and active HIGH inputs.

(4) Briefly describe the following flip-flop timing parameters:

- (a) set-up time and hold time;
- (b) propagation delay;
- (c) maximum clock frequency.

(5) Draw the circuit of a J-K flip flop using NAND gates building blocks. Verify using karnaugh maps that J-K flip-flop satisfy the characteristic equation: $Q_{n+1} = J \cdot \overline{Q}_n + \overline{K} \cdot Q_n$

(6) Apply the J-K and CLK waveforms to a flip-flop shown in Fig. 5-113. Assume that *Q = 0* initially. Sketch the output waveform.

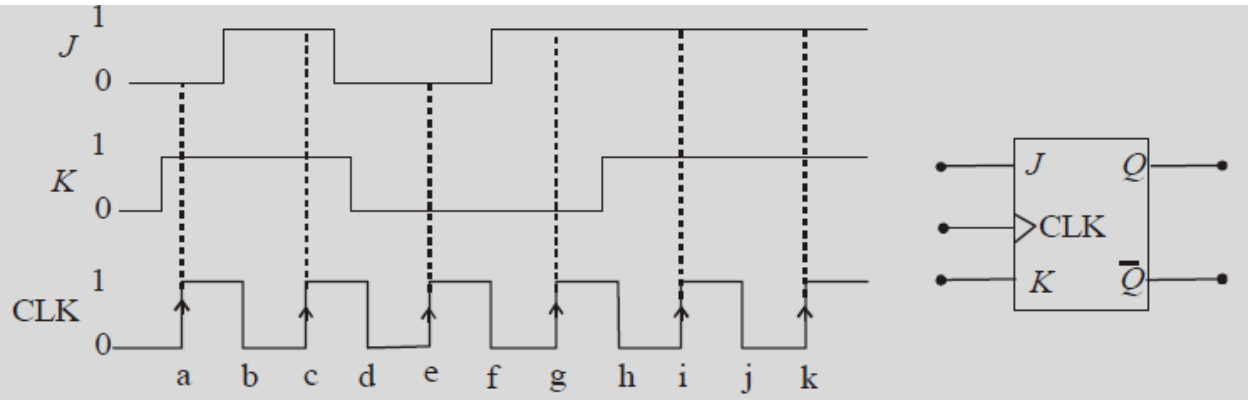

Fig. 5-113.

(7) An eight-bit binary ripple UP counter with a modulus of 256 is holding the count 01111111. What will be the count after 135 clock pulses be? (show your working)

(8) The flip-flops used in a four-bit binary ripple counter have a HIGH-to-LOW and LOW-to-HIGH propagation delay of 25 and 10 ns respectively. Determine the maximum usable clock frequency of this counter.