

Assignment 4

1. Determine the number of half and full adder circuit blocks required to construct a 64-bit binary parallel adder. Also, determine the number and type of additional logic gates needed to transform this 64-bit adder into a 64-bit adder–subtractor.
2. Design a 2-bit magnitude comparator showing the circuit implementation only.
3. Under what circumstances would you use a half-adder instead of a full- adder circuit?
4. Explain the working of a half-adder circuit with the help of truth tables. Realize a full-adder using half-adders.
5. Show that a full subtractor can be constructed using two half subtractors and an OR gate.
6. Design an 8:1 multiplexer and explain how it works. Distinguish between Multiplexer and Encoder.