Digital Electronics

Sequential Logic

Sequential Circuits

- A sequential circuit is any digital design whose output is a function of present state and the past state.
- Latches and flip-flops are the two basic circuits that have two stable states and one metastable state,
- Latches and flip-flops are also known as bistable elements capable of storing information

Bistable element

- The simplest sequential circuit is a bistable element, which is constructed with two inverters connected sequentially in a loop,
- It has no inputs and has two stable outputs labeled Q and Q’ (that is why it is called a bistable).
- However Q will take what ever value when ever the circuit is turned on.

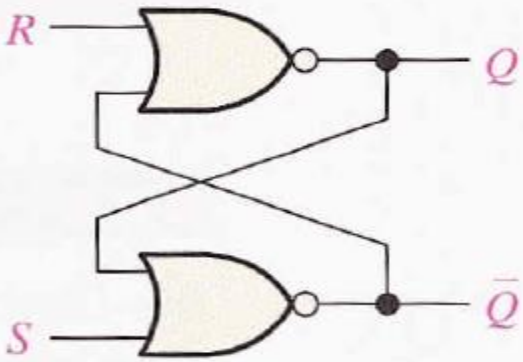
Analysis of Bistable element

- We can analyse a bistable element digitally,
- We can still analyse the bistable element by analog method.

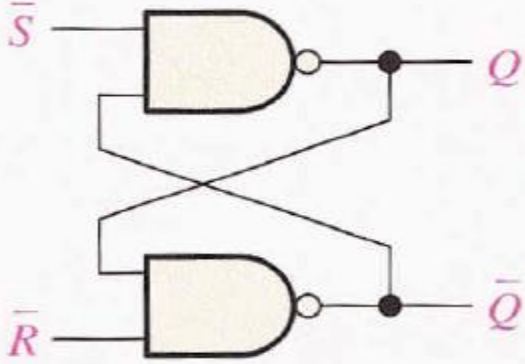
Examples of Sequential Circuit Design

- Latches (gated with enable input)
- Flip-Flops (edge triggered – synchronised or asynchronised)
- Applications:
  - Counters
  - Frequency Division
  - Registers (Storage)
  - Shift Registers
  - Debouncer

SR-Latch



(a) Active-HIGH input S-R latch



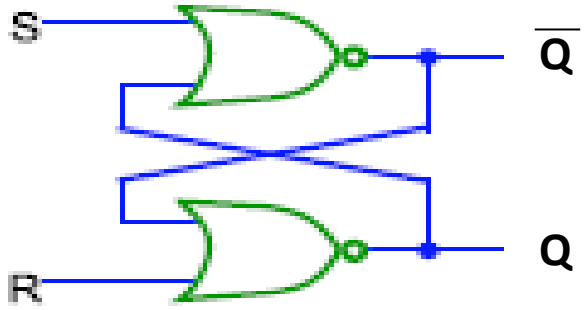
(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

S	R	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

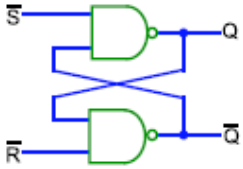
S	R	Q	$\bar{Q}$
1	1	Q	$\bar{Q}$
0	1	1	0
1	0	0	1
0	0	1	1

S-R latch (Active-High)

S	R	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	0	0	0	1
0	0	1	1	0
0	1	0	0	1
0	1	1	0	0
1	0	0	1	0
1	0	1	1	0
1	1	0	0	0
1	1	1	0	0



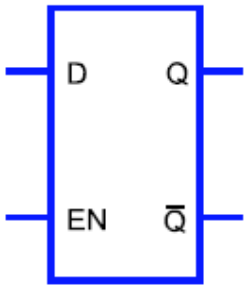
You can also get Active-Low S-R latch using NAND gates or using OR gates with negated inputs



S-R latch (low and high) has unpredictable and metastability problem.

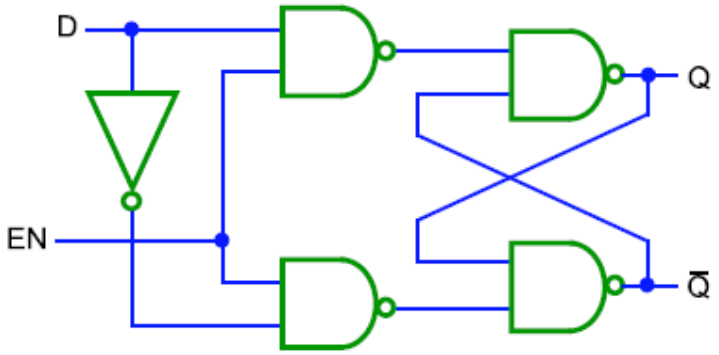
D Latch and D Latch with Enable input

- The gated D latch eliminates the invalid condition of the S-R latch. It has only 1 input and the enable input. This ENABLE input must be HIGH for the latch to change state



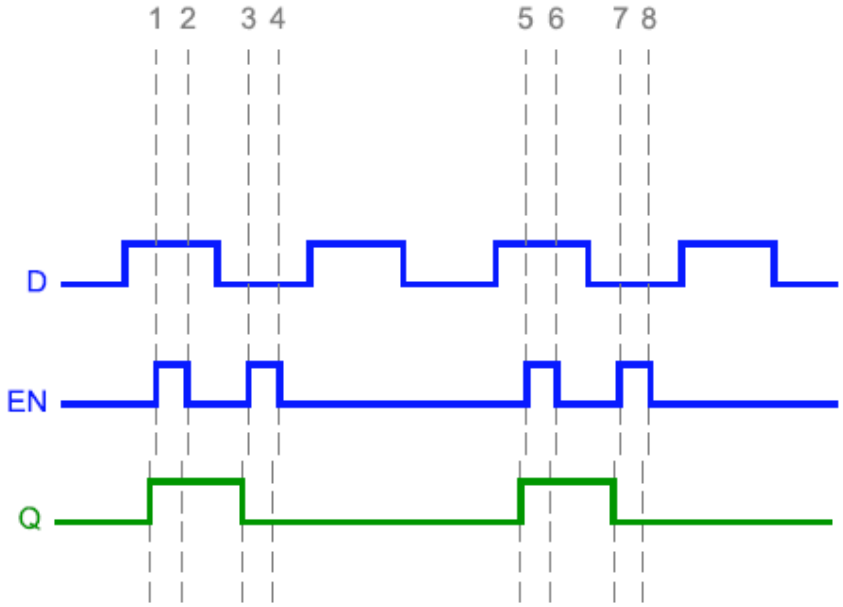
D	Q_{n+1}
0	0
1	1

Q FOLLOWS D WHEN ENABLE IS HIGH.



Example - **D Latch with Enable input**

- Sketch the Q output of a gated D latch in relation to the inputs (D and EN)



Problem: signals can propagate from a latch output to another latch's input while the clock sig

FLIP-FLOPS

- Flip-flops are synchronous bistable devices.
- There are also known as multivibrators.
- The term synchronous means that the output changes state only at a specified point on the triggering input called the clock(CKL).
- Thus changes in the output will do so in synchronism with the clock.

An Edge-Triggered Flip-Flop

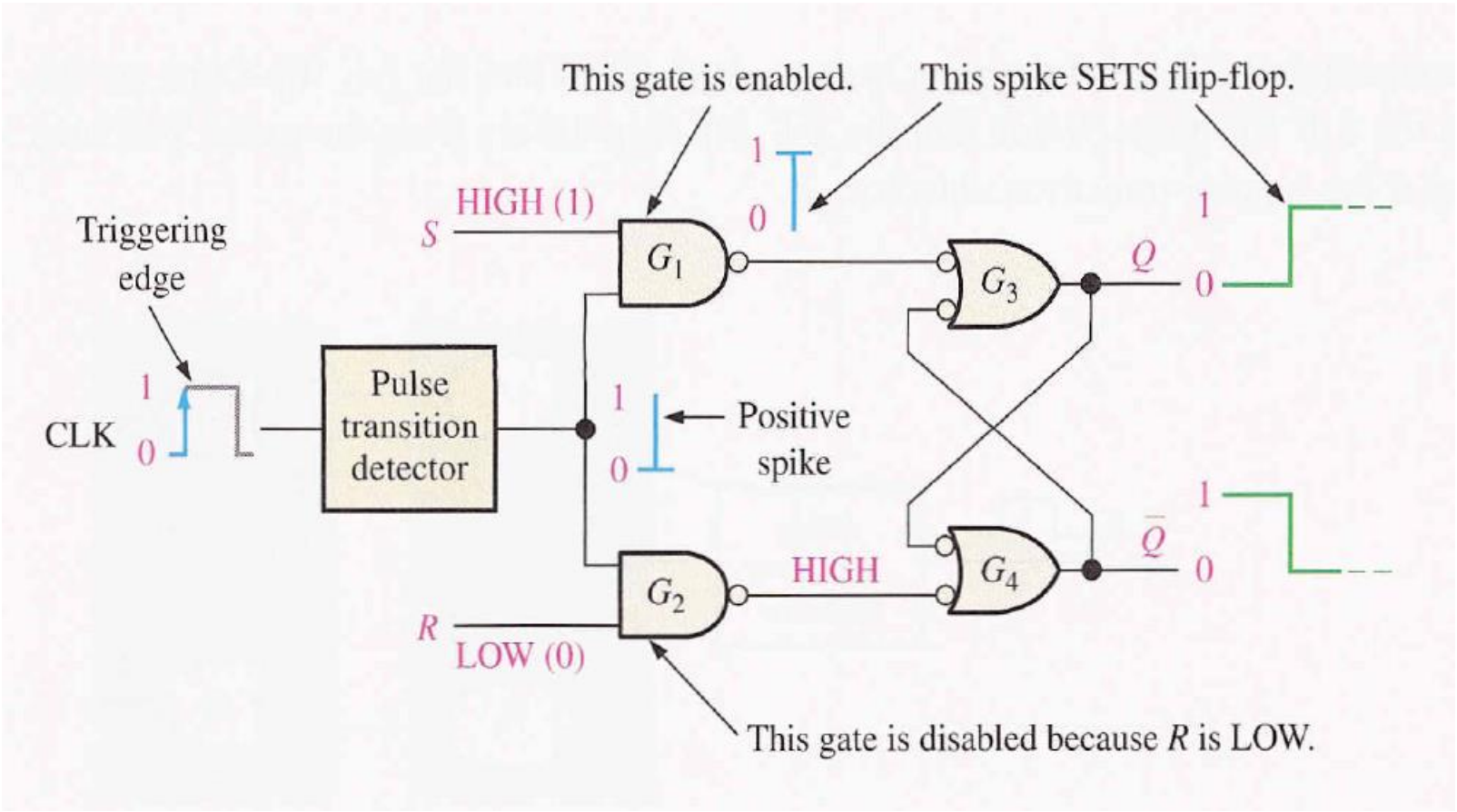
- Changes state either at the positive edge(rising edge) or at the negative edge(falling edge) of the clock pulse.
- Three types of flip-flops are covered:

✓S-R Flip-Flips

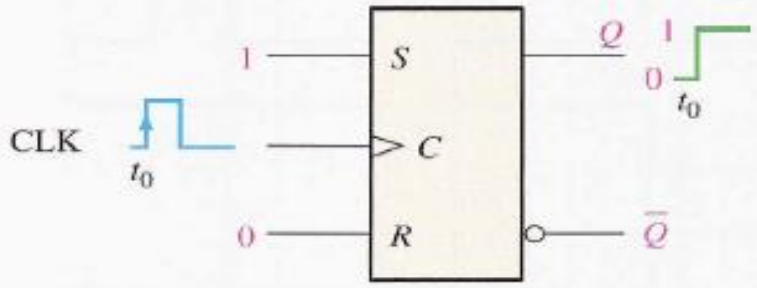
✓D Flip-Flops

✓J-K Flip-Flops

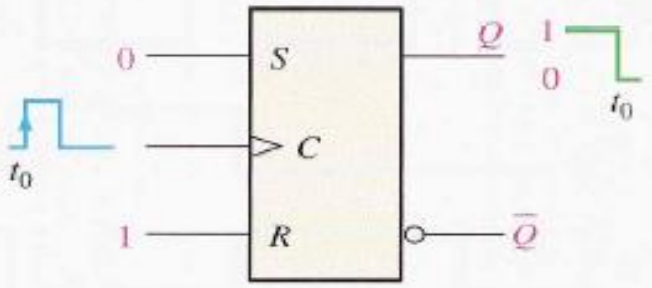
EDGE TRIGGERED SR-Flip Flop



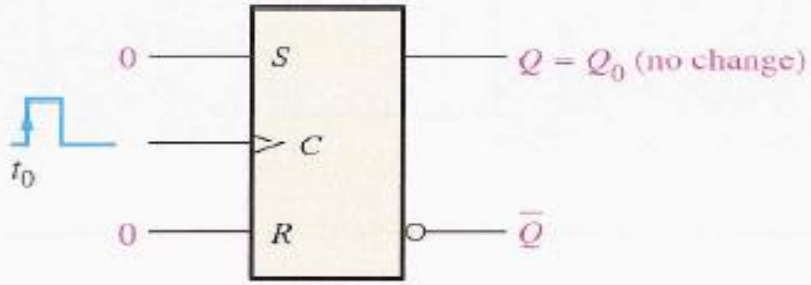
EDGE TRIGGERED SR-Flip Flop (Conti)



(a) $S = 1, R = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $S = 0, R = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)



(c) $S = 0, R = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

SR- Flip-Flop Truth Table

INPUTS			OUTPUTS		
S	R	CLK	Q	$\overline{Q}$	COMMENTS
0	0	X	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

↑ = clock transition LOW to HIGH

X = irrelevant ("don't care")

Q_0 = output level prior to clock transition

Exercise1

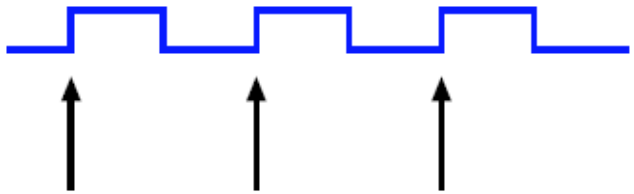
- Determine the Q output waveform of the S-R flip-flop. Assume positive edge triggering and the initial state is in RESET.

Edge-Triggered D Flip-Flops

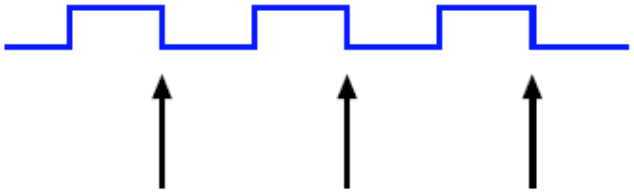
One way to design an edge-triggered D Flip-flop is to use two D latches .

In the case of a flip-flop, the triggering input is the **CLK**, or clock input. Changes in the output of a flip-flop occur in synchronisation with the clock. they change state on the positive (rising edge) or negative (falling edge) of the clock. They are only sensitive to the inputs at this edge.

- Positive Edge-Triggered

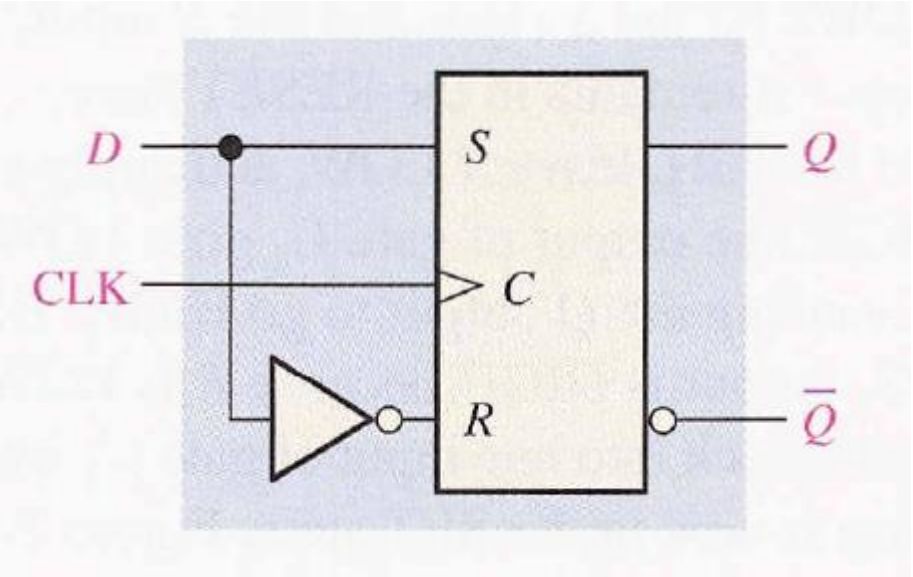


- Negative Edge-Triggered



Edge Triggered D Flip-Flops

- The D flip-flops is useful when a single data bit (1 or 0) is to be stored. The addition an inverter creates a basic D flip-flop.



Truth Table for D Flip-Flops

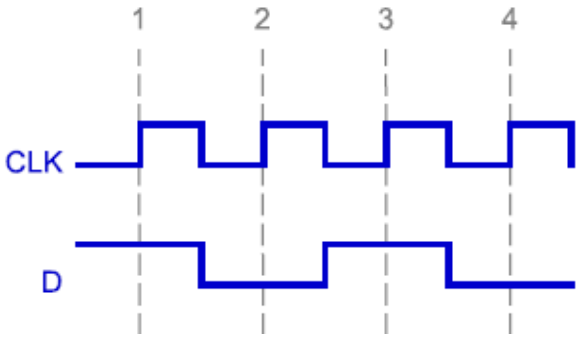
- Q follows D at the triggering point of the clock

INPUTS		OUTPUTS		
D	CLK	Q	$\overline{Q}$	COMMENTS
1	↑	1	0	SET (stores a 1)
0	↑	0	1	RESET (stores a 0)

↑ = clock transition LOW to HIGH

Exercise2: positive edge-triggered D flip-flop

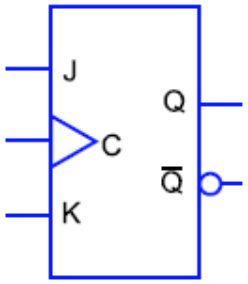
- Draw the output waveform for the inputs given at every rising edge of the clock.



J-K Flip-Flops

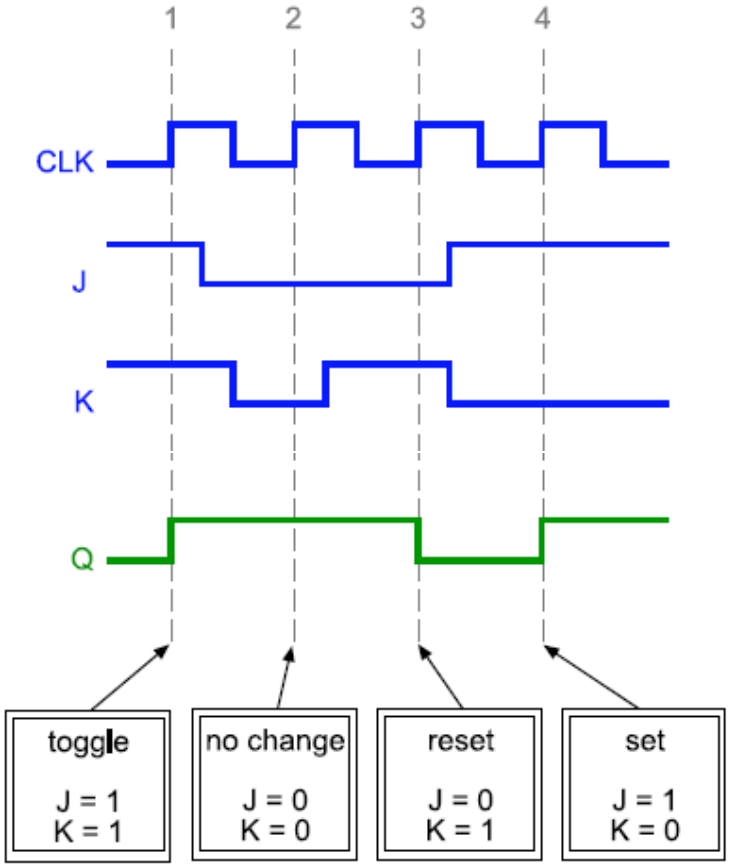
- The J-K flip-flop is versatile and is widely used type of flip-flop.
- The functioning of the J-K flip-flops is identical to that of S-R flip-flops in the SET, RESET, and NO CHANGE conditions of operation.
- The difference is that the J-K flip-flop has no invalid state as does the S-R flip-flop.

Edge-Triggered J-K Flip-Flop



J	K	C	Q_{n+1}	$\overline{Q_{n+1}}$	Effect
0	0	↑	Q_n	$\overline{Q_n}$	No change
0	1	↑	0	1	Reset
1	0	↑	1	0	Set
1	1	↑	$\overline{Q_n}$	Q_n	Toggle

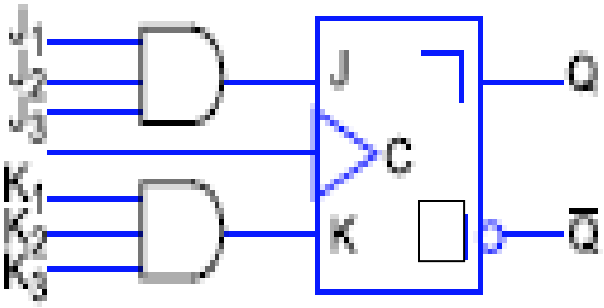
Calculate the output waveform given the input waveforms. Assume the flip-flop is initially reset.



Exercise3 – **Edge-Triggered** J-K Flip-Flop

The following serial data is applied to the flip-flop as indicated in the table and
the figure. Determine the resulting serial data that appear on the Q output. There is only one clock pulse for each bit time. Assume that Qn is initially 0. Right-most bits

J_1	1010011	K_1	**1001110**
J_2	0111010	K_2	1101100
J_3	1111000	K_3	1010101



Asynchronous Inputs

- Synchronous: inputs and are transferred only to the output when the flip-flop is triggered by the clock edge.

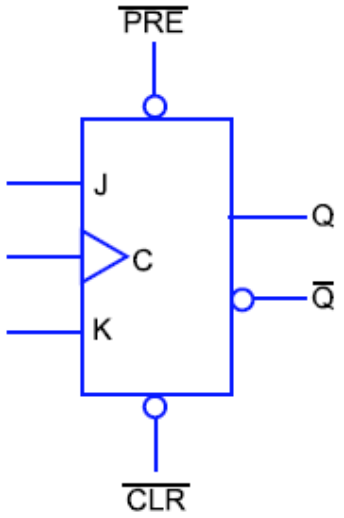
- Asynchronous: effects are independent of the clock. The normal asynchronous inputs are preset (PRE) and clear (CLR).

- When $\overline{PRE}$ is LOW, the device will preset the output Q to a 1.

- When $\overline{CLR}$ is LOW the device will clear and the output Q will be 0.

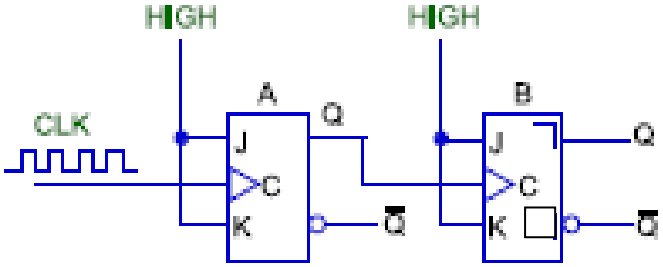
- $\overline{PRE}$ and $\overline{CLR}$ must be high for the flip-flop to function normally.

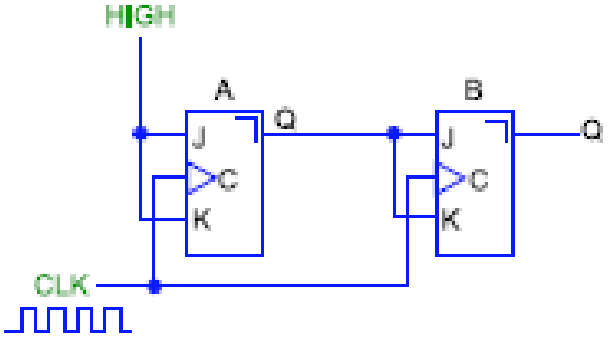
- $\overline{PRE}$ and $\overline{CLR}$ override the synchronous inputs

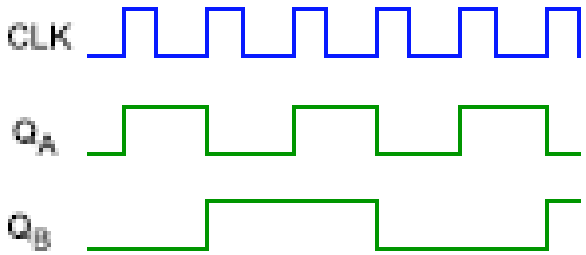


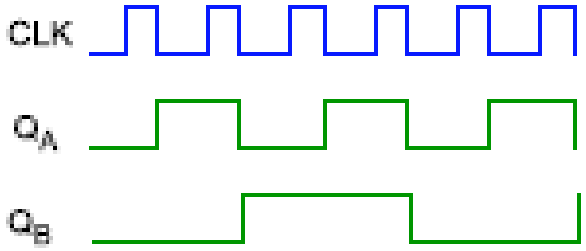
Example – **Synchronous and Asynchronous Flip-Flops**

Sketch the Q output of flip-flop B in proper relation to the clock for both cases. The flip-flops are initially reset.



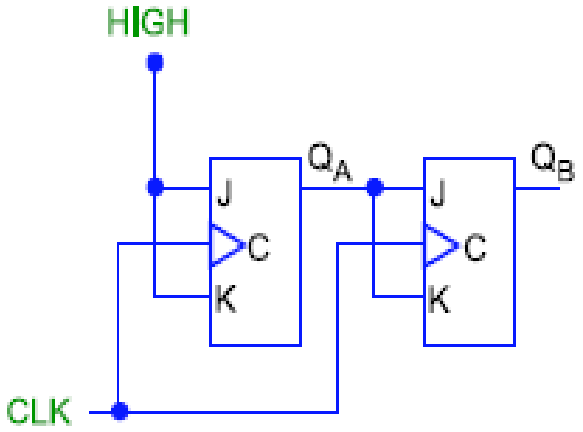






Application 1: Synchronous Counters

- **Same clock connected to all flip-flops**
- **Clocked simultaneously**



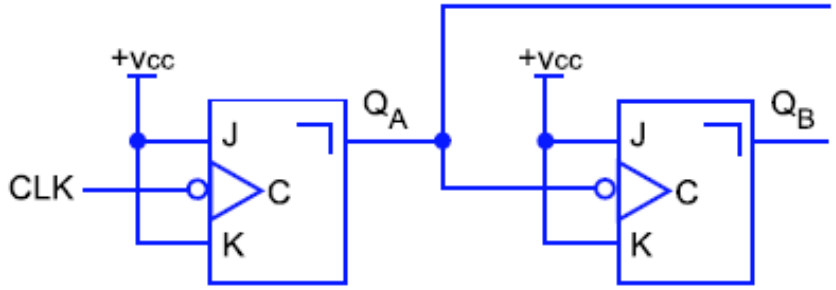
Ex: Sketch waveforms for 2-bits a synchronous counter

Clock Pulse No.	Q_A	Q_B
1	$0 \rightarrow 1$	$0 \rightarrow 0$ (no change)
2	$1 \rightarrow 0$	$0 \rightarrow 1$ (toggle)
3	$0 \rightarrow 1$	$0 \rightarrow 0$ (no change)
4	$1 \rightarrow 0$	$0 \rightarrow 1$ (toggle)
5 (1)	$0 \rightarrow 1$	$0 \rightarrow 0$ (no change)

Clock Pulse No 3 should be 1→ 1
Clock pulse no 4 should be 1→ 0

Application 1: **Asynchronous Counters**

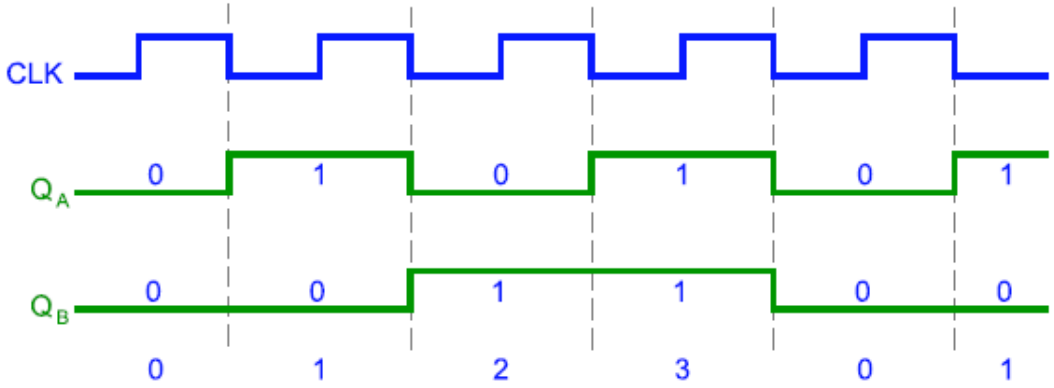
First flip-flop clocked by the external clock, all other flip-flops are clocked by the output of the previous flip-flop (not clocked simultaneously)



Sequential counter using a lock-out J-K flip-flops

2 bits – counts 0 to 3

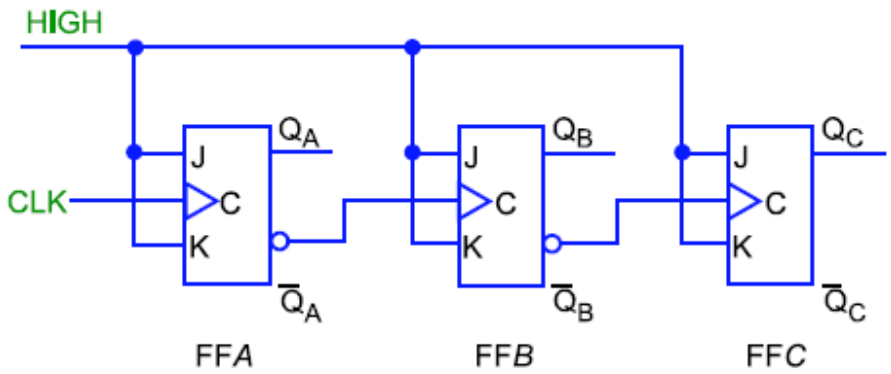
This is the same circuit as for the frequency division !?

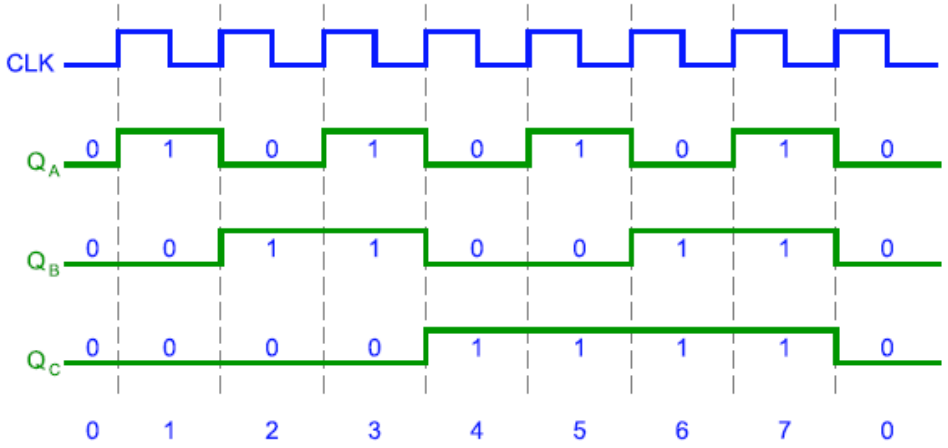


Application 1: **Asynchronous Counters**

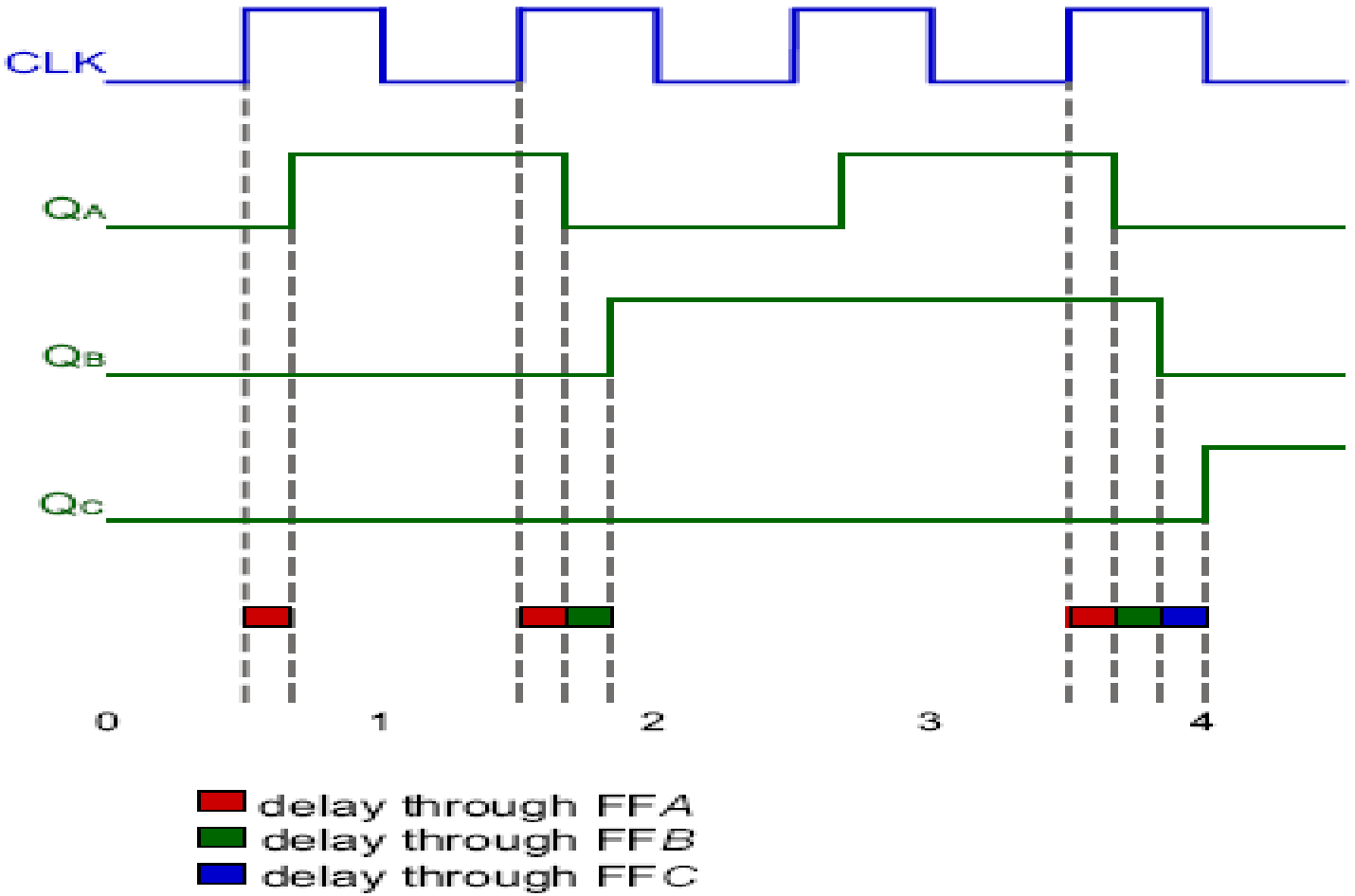
Sequential counter using $\overline{Q}$

3 bits – counts 0 to 7





Propagation delay in the Asynchronous (ripple) Counters



Example - Propagation delay

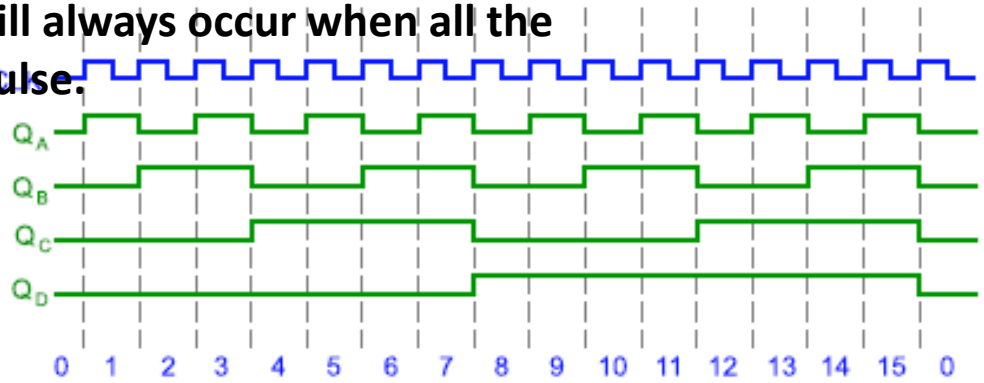
Say 5 ns delay for each FF.

First change is on the 8th clock pulse - change in signal must go through all 4 flip-flops.

Total delay until Q_D changes is 4*5ns=20ns .

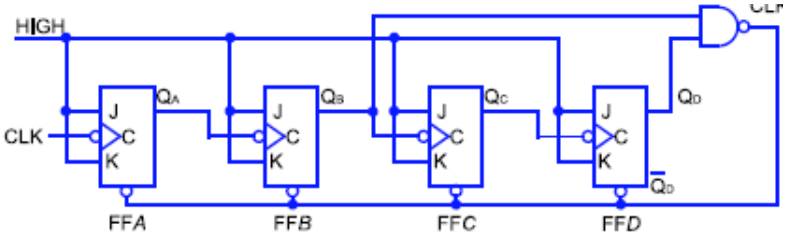
The longest delay that occurs in this counter as all 4 flip-flops change at once.

The longest possible delay will always occur when all the flip-flops change one clock pulse.



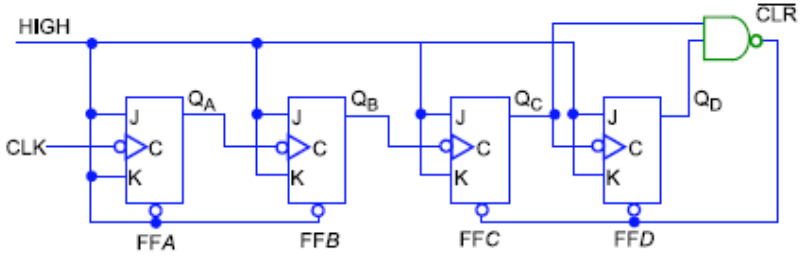
Modulus and Truncated Counters (decade counter)

- **They are less than 2^n counters. Usually 10 (0 to 9) or 12.**
- **To construct a decade counter we must force the counter to recycle before going through all of the normal states.**



1010_2 ($D\overline{C}B\overline{A}$)

Example: create a modulus 12 counter using J-K flip-flops



1100_2, or $DC\overline{BA}$.

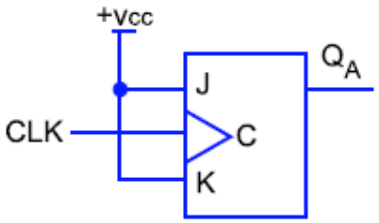
Other Counters

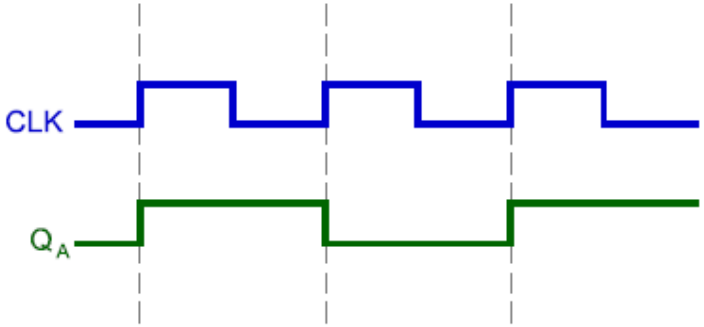
1. Up/Down Counters
   - bi-directional counter - can count either up or down
   - most can be reversed at any point in the counting sequence

2. Cascade Counters
   - connect counters in cascade to achieve higher modulus
   - last stage of output of one counter drives the input of the next

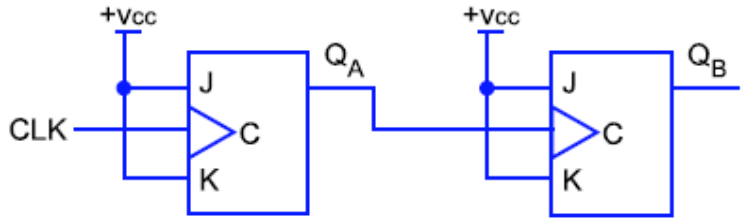
Application 2 : **Frequency Division**

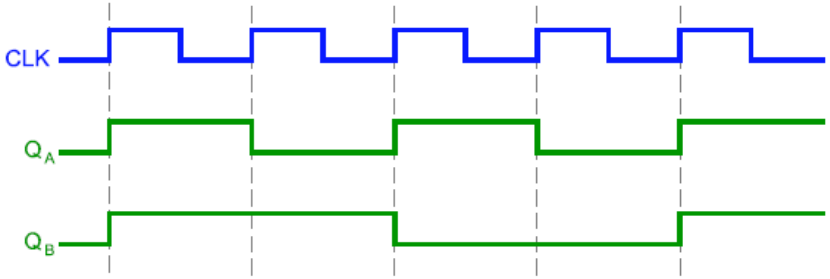
- J-K Flip-flops can be used to divide the frequency of the input clock waveform.





Frequency Division by 2





Also counter 3

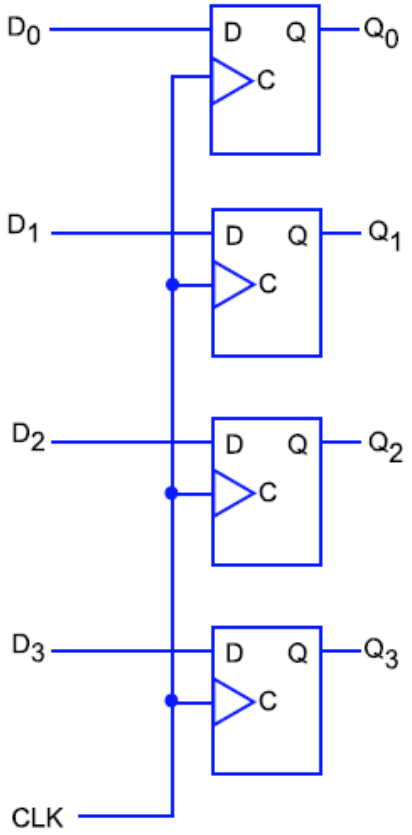
3 2 1 0

Frequency Division by 4

Application 3 : Registers (storage)

D flip-flops can take data in on parallel lines and store it simultaneously. Each flip-flop is triggered at the same time, as all are connected to the same clock input.

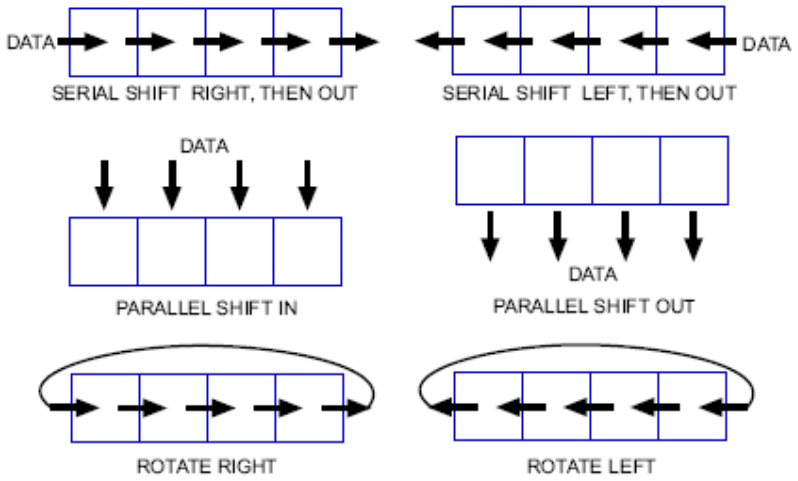
Parallel In/Parallel Out



Other Registers : Shift Registers (data transfer)

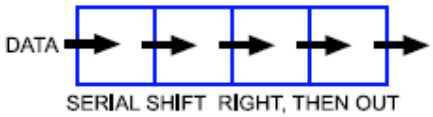
The storage capacity of a shift register is the number of bits of data it can retain

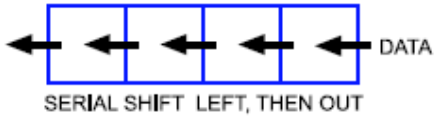
- **Several types**
  - Serial In/Serial Out
  - Serial In/Parallel Out
  - Parallel In/Serial Out

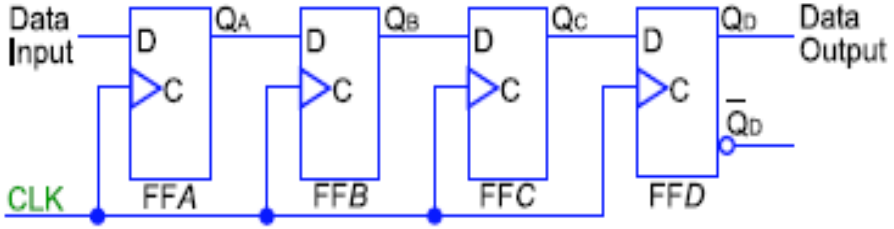


Serial In/Serial Out Registers

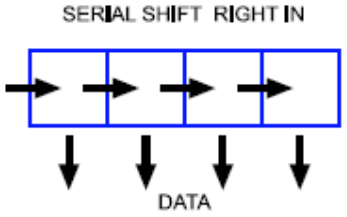
- On first clock Data -> Q_A
- On next clock $Q_A \rightarrow Q_B$
- On next clock $Q_B \rightarrow Q_C$
- On next clock $Q_C \rightarrow Q_D$

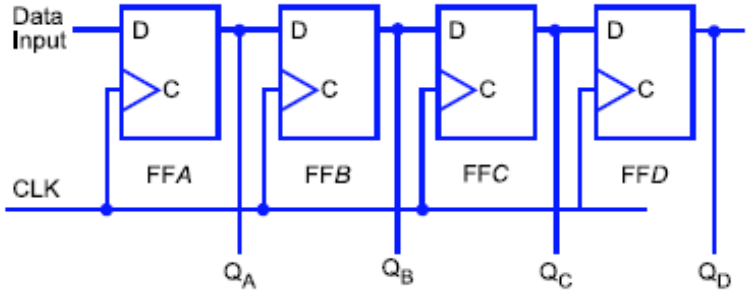




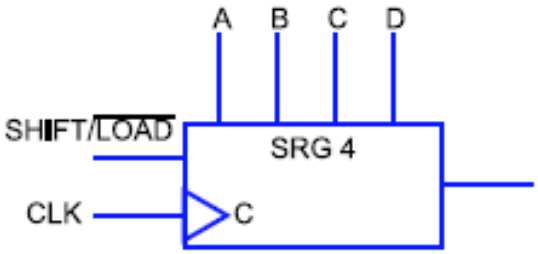


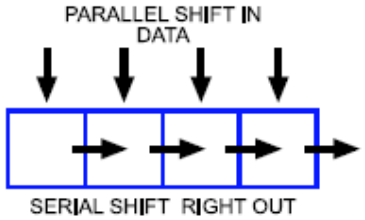
Serial In/Parallel Out Registers

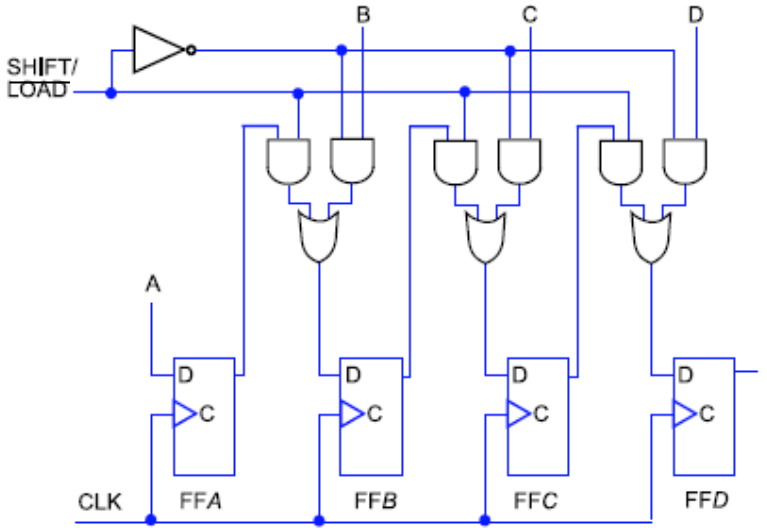




Parallel In/Serial Out Registers







When the input is high the shift register shifts the data serially

When this input is low the data is loaded into the register in parallel.

END