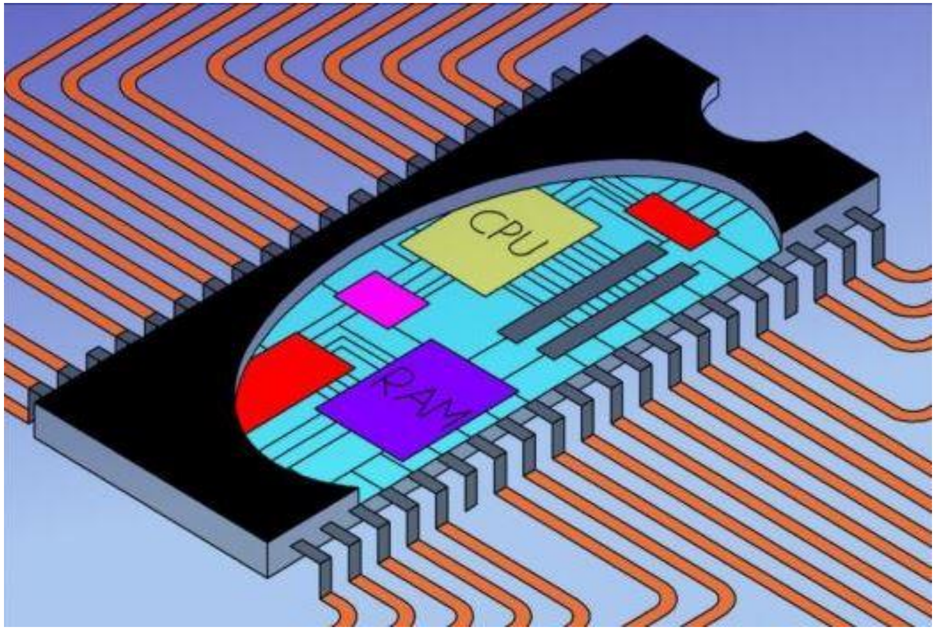
The University of Zambia

EEE 3131 – DIGITAL ELECTRONICS



Jasper HATILIMA

Department of Electrical and Electronic Engineering, School of Engineering

jasper.hatilima@unza.zm
jasperhatilima@yahoo.com

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Course Outline

Jerry Muwamba

Number Systems and Codes

Logic Fundamentals

Combinational Logic

Jasper Hatilima

Logic Families:

- Logic Families, TTL, ECL, CMOS

Sequential Logic Circuits:

- S-R latch, Clock S-R Flip Flop, Level and Edge Triggering, J-K, D-Flip Flops, State Tables, State Diagrams.
- Serial/Parallel In/Out shift registers.
- Timing diagrams, Asynchronous (unclocked) and synchronous systems, Counters: ripple, synchronous, ring counters.

Introduction to Microprocessors and PLDs:

- Three State Registers.
- Memories: ROM, PROM, EPROM, EEPROM, SRAM, DRAM.
- PLAs, PALs, FPGAs, HDL
- Microprocessor Architecture, Instruction Set, Assembly language, Simple-As-Possible Computer.

Recommended Books

[1] Electronics – A Systems Approach, 3rd Ed., by Neil Storey

[2] Circuits, Devices and Systems, 5th Ed., by R.J. Smith and R.C. Dorf

[3] Introduction to Microprocessors – A. P. Mathur (Check Bookworld)

[4] Basic Electronics – Devices, Circuits and IT Fundamentals by S. Kal

[5] Digital Computer Electronics, 3rd Ed., by A. P. Malvino & J. A. Brown

Pretty much any “recent” book on electronics ☺

MINIMUM REQUIREMENTS (CA):

- ❖ 6 Labs (3hrs each) : 15%
- ❖ 8 Assignments: 5%
- ❖ 1 Test (2 hours): 20%
- ❖ 1 Final Exam (3 hours): 60%

PREREQUISITES:

EEE 3571 – Electronic Engineering I

SOFTWARE TOOLS:

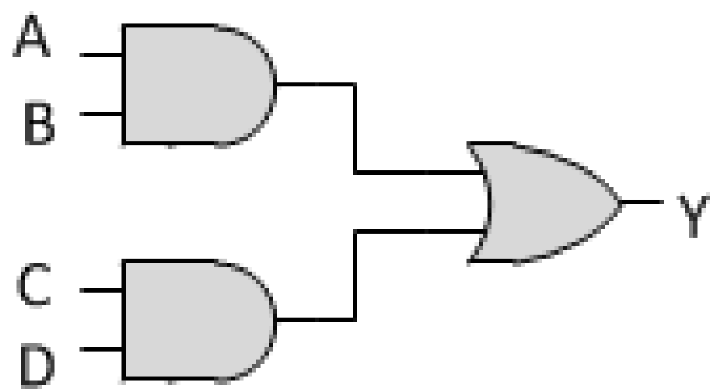
- ✓ Multisim
- ✓ VHDL

Logic Families

At the end of this component, the student should:

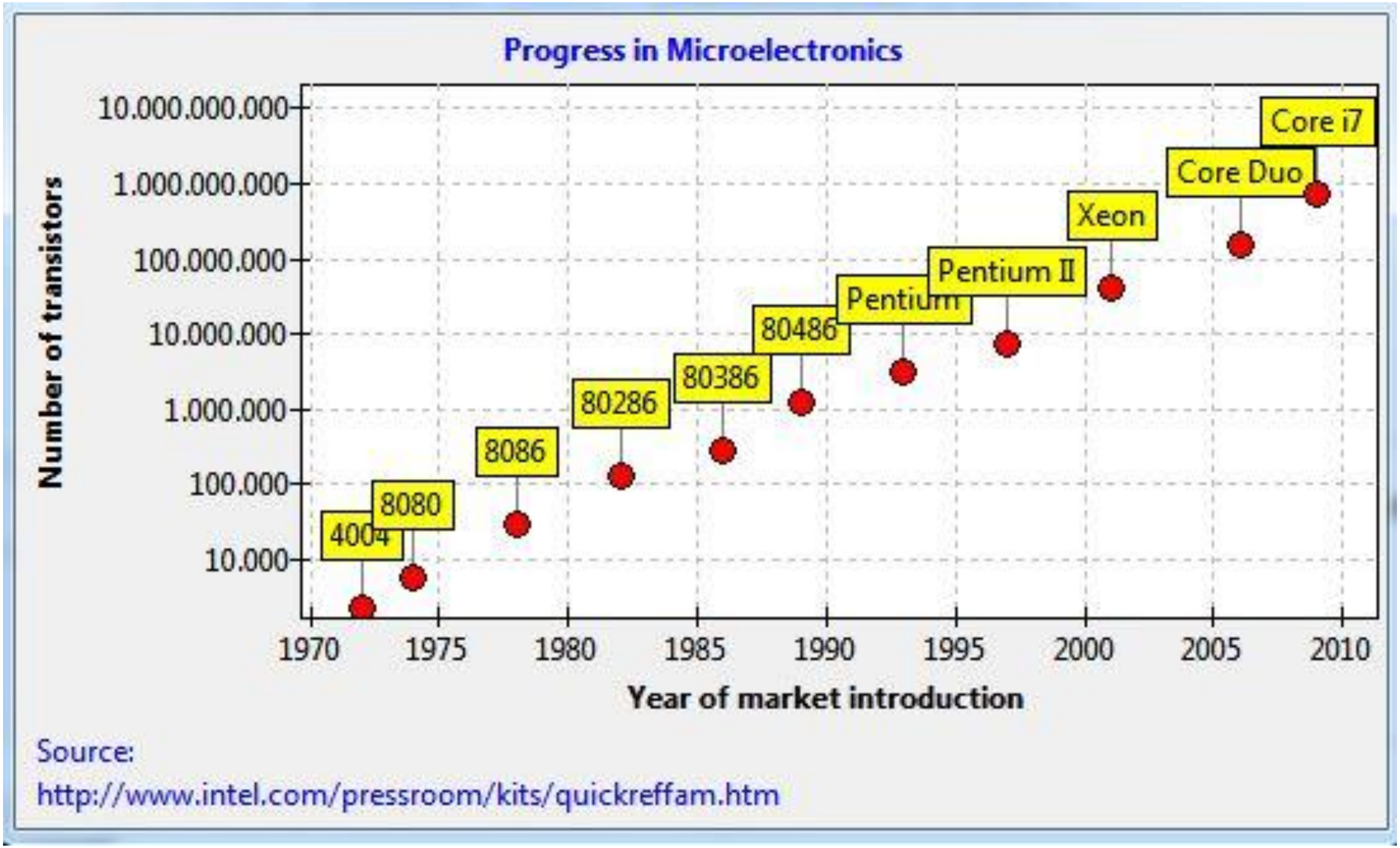
- ❖ be aware of basic implementation of logic gates using transistors and diodes.
- ❖ understand the commonly used families of digital IC logic.
- ❖ understand the advantages and disadvantages of each logic family.

INTRODUCTION



- In the analogue course (EEE3571), we introduced electronic engineering and focused on the analogue aspects.
- We mainly focused on the transistor as a discrete component and the only time we used it in an integrated circuit was in the analogue IC for an Op-Amp.
- The EEE3571 required operation of the transistor within the linear region.
- We now move to an even higher level of integration and will operate the transistors involved in the other two regions of the output characteristics.
- Recall Moore’s law: Number of transistors per chip doubles every 1.5 to 2 years

$$SSI \leq 100 < MSI \leq 1{,}000 < LSI \leq 10{,}000 < VLSI$$


Progress in Microelectronics
Number of transistors
10.000.000.000
1.000.000.000
100.000.000
10.000.000
1.000.000
100.000
10.000
1970
1975
1980
1985
1990
1995
2000
2005
2010
Year of market introduction
4004
8080
8086
80286
80386
80486
Pentium
Pentium II
Xeon
Core Duo
Core i7
Source:
http://www.intel.com/pressroom/kits/quickreffam.htm

A BUILD UP ON LAST TERM:

- Last term, you learnt about **number systems, logic gates and Boolean algebra**. We are now going to go into the gates and then out again.

- It is important at this point to know the various **logic families used in implementing the basic logic gates**. This will give us an understanding of the **characteristics of the ICs implemented using certain families** **(speed, power, noise)**.

- We will use the tools from the previous lectures to come up with **implementation of useful digital electronic circuits / ICs (combinational and sequential)**. **IC numbering for TTL to be done.**

- For each ‘sub-system’ done, it will be important to **select a TTL IC that performs the specific function**. This will help us to easily reference a specific IC as **we progressively develop a functional microprocessor based system**.

Logic Families

- With manufacturers being able to miniaturize circuits using advanced photographic techniques on semiconductors, the final circuits are **small**, **low cost** (economies of scale), **highly reliable** (simultaneous fabrication) and **high speed**.

- The final circuit is so small that you would need a microscope to see the connections. The circuit is called an **INTEGRATED CIRCUIT** (IC) because the components are an integral part of the chip (Inside the ceramic substrate packaging).

- The integrated components can be resistors, diodes, transistors and even small capacitors.

Different combinations of the above components form different logic/digital families...

A **digital family** is a group of compatible devices with the same logic levels and supply voltages. This means that you can connect the output of one of the devices to the input of the other.

Logic families are divided into two:

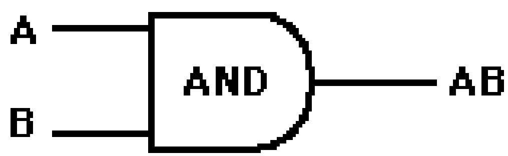
- ✓ **Bipolar Families**
- ✓ **MOS families**

In the next section, we will focus on the Bipolar families and then we will just give a little insight into the MOS families. After that, we will revert back to a commonly used family within the Bipolar category, TTL. What will be learnt under TTL can easily be used with others.

Families from the BIPOLAR CATEGORY:

1. Diode Logic (DL)

- ✓ Simplest but scaling not easy.
- ✓ Cannot perform INVERSION (NOT).
- ✓ Only has historical significance.



Implemented as:

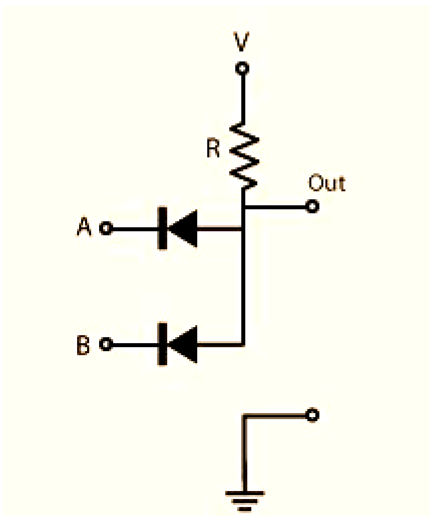


Fig. 1.1 DL

2. Resistor-Transistor Logic (RTL)

- ✓ Scaling is easy.
- ✓ Though has large power consumption.
- ✓ Only have historical significance.

Implemented as:

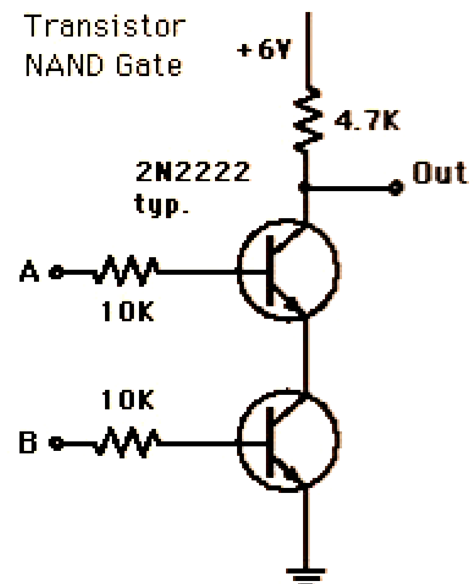
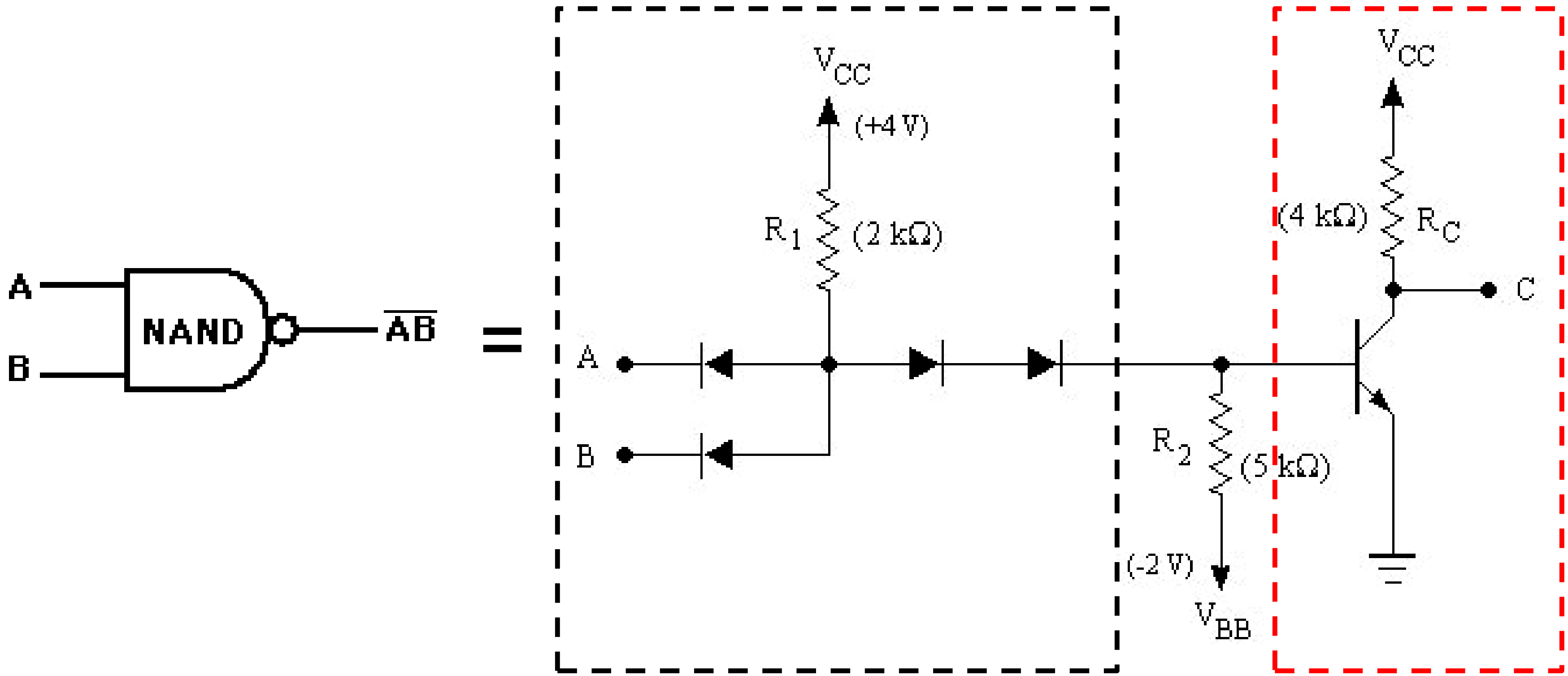


Fig. 1.2 RTL

3. Diode–Transistor Logic (DTL)

- ✓ This in essence is diode logic with transistor amplification.
- ✓ Reduced power consumption.
- ✓ Faster than RTL.



Diode Logic AND gate

Saturating Inverter

Fig. 1.3 DTL

4. Transistor-Transistor Logic (TTL)

Physical construction of ICs made it more effective to replace the diodes at the input of a DTL gate with Multi-Emitter input Transistors. This became the standard logic circuit in most applications for many years.

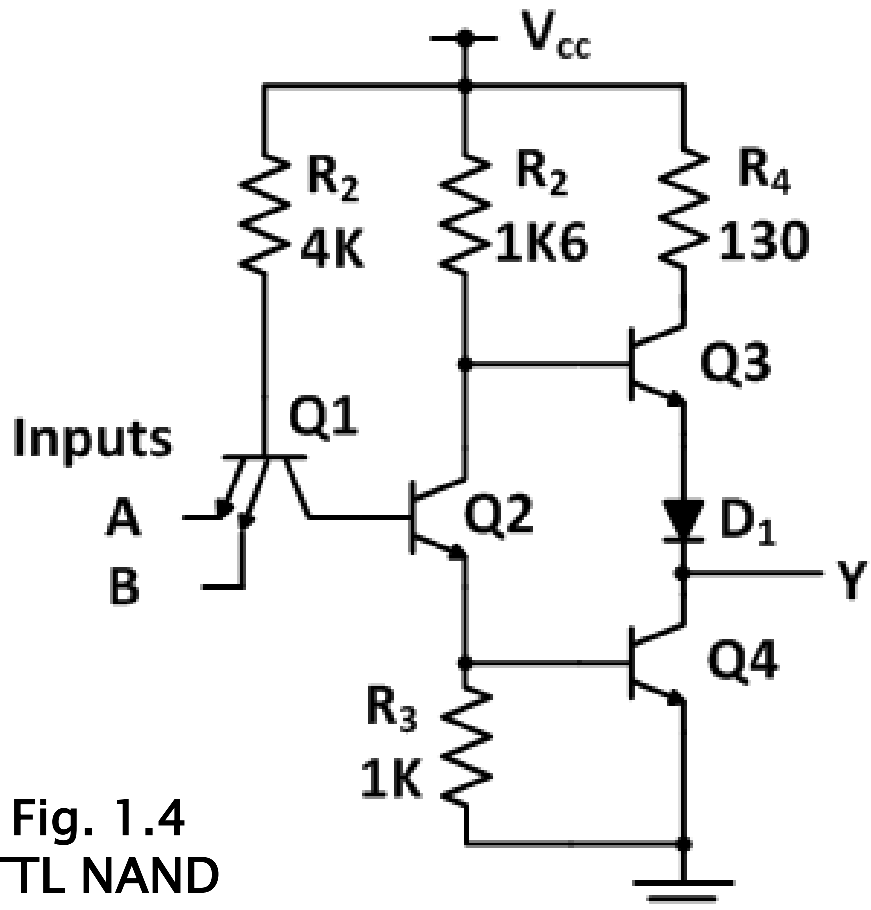


Fig. 1.4
TTL NAND

TTL NAND Key Features:

- ✓ Multi-emitter input transistor Q1.
- ✓ Totem-Pole Output made up of Q3/Q4 (Push-Pull config.)
- ✓ Diode D1.

All the above three are described below...

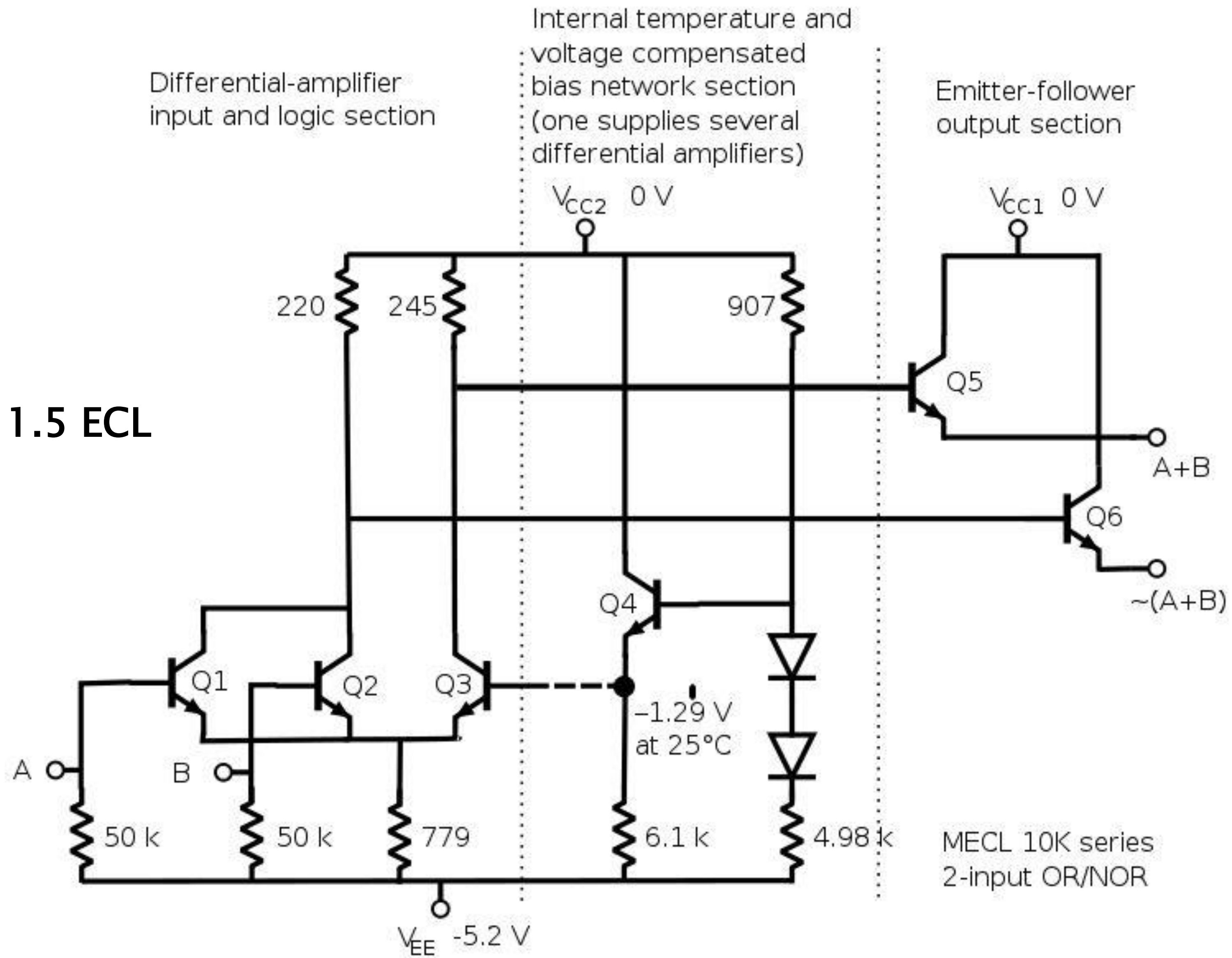
- ✓ **The multi-emitter input transistor** is a special design such that each emitter acts like a diode. This makes Q1 and the 4K resistor to act like an AND gate. This kind of transistor requires less area on the silicon wafer during fabrication and therefore results in relatively faster speeds of operation.

✓ **The Totem-pole** has advantage of low output impedance either as Emitter follower or as Ground and therefore low time constants when connecting to the next stage.

✓ **The Diode D_1** ensures that Q3 does not conduct when output is low. Its voltage keeps the base-emitter diode of Q3 in reverse biased mode.

5. Emitter-coupled Logic (ECL)

Fig. 1.5 ECL



ECL

- ✓ Notice the coupling of the emitters in the differential pair in logic section. Any small difference between input and reference voltage will cause the output to swing either positive or negative (high/low). Thus small logic voltage swings (0.8V or less!). **Check noise susceptibility** **and** **Side Channel Attack**.
- ✓ Constant current source provided by the NEGATIVE VOLTAGE and the resistor in the emitter of the differential pair. This current is made smaller than saturation current hence no saturation of the BJTs and thus FASTER SWITCHING SPEEDS.
- ✓ Large output currents in the Common Collector outputs.

Compare with TTL in terms of power supply, switching speed, power consumption and logic levels.

Families from the MOS CATEGORY:

Do a quick reading on MOSFETs. One of the things you will find is that they are voltage controlled elements. But most importantly, the following are the MOS families:

1. PMOS

- ✓ Made from p-Channel MOSFETs.
- ✓ Oldest of the MOS category and slowest; thus **Obsolete**.

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2. NMOS

- ✓ Made from n-Channel MOSFETs.
- ✓ Found use in Memories and Microprocessors in LSI.
- ✓ Also **obsolete**.

3. CMOS – Complimentary MOS

A push-pull of p-Channel and n-Channel MOSFETs.

✓ Simple to fabricate

✓ Current only flows when input is changing from one state to another. Therefore **lower static power consumption** compared to Bipolar families which consume power even when doing nothing.

✓ Due to low heat generated, billions of MOS transistors can be packed on a single chip: **High packing density**.

Because of the advantages above, CMOS devices have become dominant in manufacturing of ICs.

Extensively used in portable devices where low power consumption is desired/Battery-powered applications.

Anything bad about CMOS?

Disadvantages of CMOS

✓ Not as fast switching as ECL.

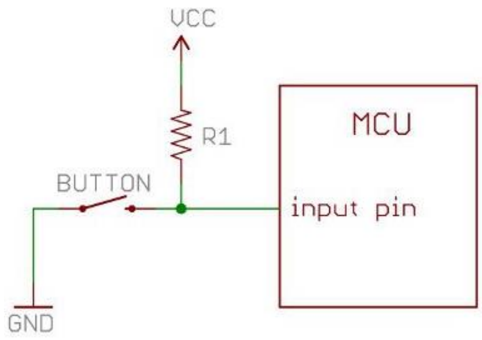
✓Susceptibility to Electrostatic Discharge (ESD).
Recall ESD attack in some movies ☺

✓ Latch-Up: Parasitic circuit effect where there is a short circuit between V_{DD} and Ground usually resulting in chip destruction (or system failure requiring restart). Latch-up prevention is a challenge for both process engineers and circuit designers.

ONE THING ABOUT CMOS INPUTS:

Never leave CMOS input floating!

Unused inputs must be pulled-up to some fixed voltage level.



FYI:

Below is the naming and evolution of CMOS family:

EVOLUTION

SERIES	FEATURES
4000	High noise margin, practically obsolete.
74C00	CMOS, pin compatible with TTL. Obsolete.
74HC00/74HCT00	High speed CMOS, input voltage compatible with TTL.
74AC00/74ACT00	Advanced CMOS,
74AHC00/74AHCT00	Advanced High speed CMOS.
BiCMOS	Combining best features from Bipolar and MOS.
74LVC00/74ALVC00/ 74LV00/74AVC00	Low voltage CMOS. 5V/3.3V translation. AVC optimized for 2.5V

TTL Standard IC Naming

Two versions of TTL identified by the following series numbers:

- ✓ **5400 series**: Military version, −55º C to 125º C.
- ✓ **7400 series**: Commercial version, , 0º C to 70º C

5400 series devices can replace 7400s but cost is too high.

We will now give a bit more detailed description of various configurations of the TTL 7400 series that are used in order to optimize between power usage, switching speeds, etc.

1. Standard TTL

- ✓ Designated as **74XX** e.g. 7402 is a Quad 2-input NOR gate.

2. High Speed TTL

By decreasing the internal resistances in the standard TTL, the manufacturer can reduce the time constants and thus the propagation delay is decreased ->> **High Speed**.

But this is done at a cost: **Increased power dissipation** .

- ✓ Designated as **74HXX** e.g. 74H02 is a Quad 2-input NOR gate.

3. Low Power TTL

By increasing the internal resistances in the standard TTL, the manufacturer can reduce the power consumption.

But this is done at a cost: increased delay ->> **slower devices**.

Devices in this series have the following features:

- ✓ Designated as **74LXX** e.g. 74L02 is a Quad 2-input NOR gates.

4. Schottky TTL

- ✓ When a Schottky diode is used to clamp the base-collector Junction of a transistor, a Schottky transistor is formed;

- ✓ The base-collector voltage is limited to diode voltage and so does not saturate.

- ✓ Then using a Schottky transistor in TTL forms the fast switching **Schottky TTL**..

- ✓ Designated as **74SXX** e.g. 74S02 is a Quad 2-input NOR gates.

5. Low-Power Schottky TTL

By finding the best compromise between low power and high speed in Schottky TTL, **low-power Schottky TTL** devices are formed and designated as **74LSXX** e.g. 74LS02.

Some Special Characteristics of Logic Devices

- ✓ We have previously listed the various logic families and compared them **qualitatively**.

- ✓ At this point, it is important to **quantitatively** know some of the important logic device parameters that are key in designing digital circuits.

1. **Fan-In (FI)** of a gate is the number of inputs a gate has; e.g. a two-input AND gate has a fan-in of 2.

   Two parameters associated with the fan-in:

   ✓ I_{IH} – Input high current and

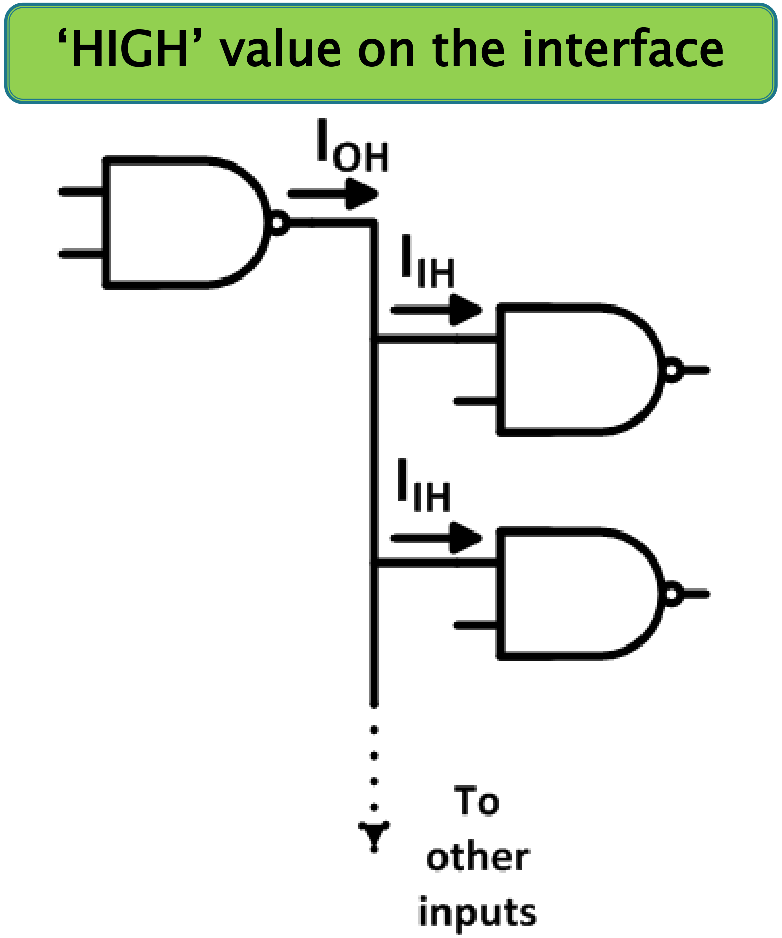
   ✓ I_{IL} – Input low current.

2. **Fan-Out (FO)** of a gate is the number of standard loads that can be connected to the output of the gate without degrading its normal operation. It is computed based on the capability of the gate to maintain logic high or low (**Logic levels will be discusses later**)

   Two parameters associated with fan-out:

   ✓ I_{OH} – current when output is high and

   ✓ I_{OL} – current when output is low.



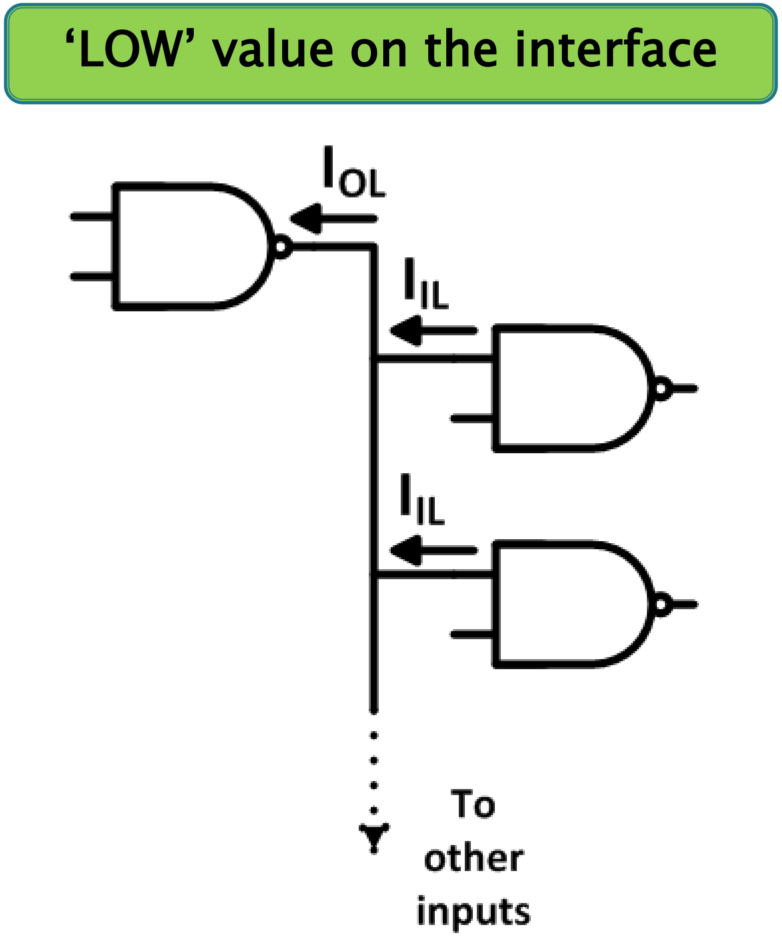


Fig. 1.6

$$FO = \min\left\{ \frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}} \right\}$$

3. **Power Dissipation** of a gate is the amount of power required to operate the gate i.e. the power delivered to the gate from the power supply.

   If the supply voltage is V_{CC} and the gate draws I_{CCL} and I_{CCH} for low and high respectively, then average power is

$$P_{Avg} = V_{CC} \frac{I_{CCH} + I_{CCL}}{2}$$

4. **Propagation Delay** is the time between the logic change on an input and the corresponding logic change on the output.

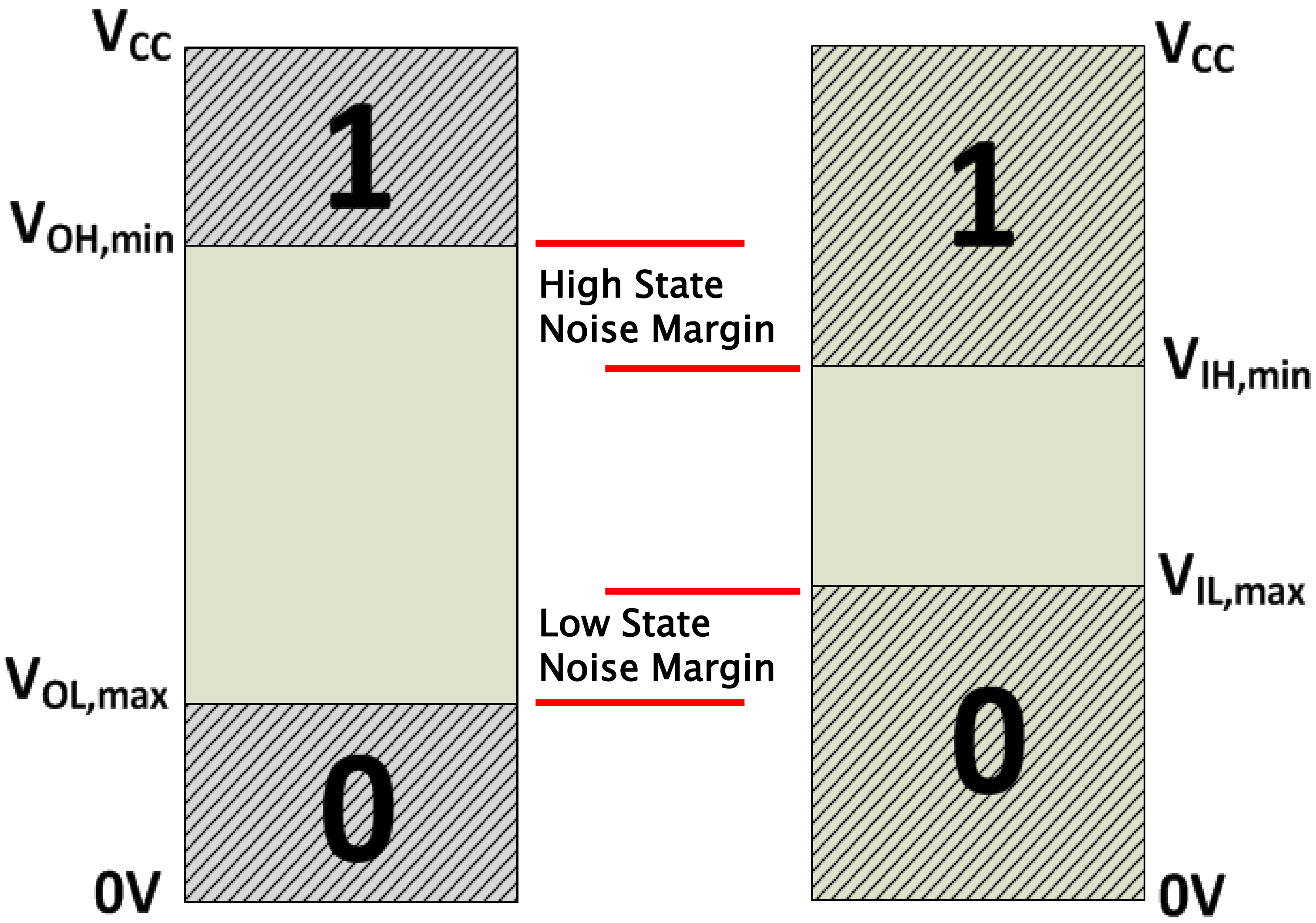
   Also note that there are other time parameters called **Rise/Fall times** and these specify the signal bandwidth to be used (given in data sheets)

5. **Noise Margin (NM)** of a gate is the maximum noise voltage that can be added to an input signal without causing undesirable outputs.

Noise comes in form of DC noise caused by voltage level drift and also from AC noise caused by random pauses of other switching circuits etc.

Noise margin is calculated using voltage levels of the input signal and output signal.

The diagram below gives an indication of the noise margin:



(a) Guaranteed Output Range (b) Recognizable Input Range

Fig. 1.7 Noise Margin

- ✓ **Low Noise Margin (LNM)** : The largest noise amplitude that can be superimposed (positively) on the low state input voltage to a logic gate without causing undesirable output.
- ✓ **High Noise Margin (LNM)** : The largest noise amplitude that can be superimposed (negatively) on the high state input voltage to a logic gate without causing undesirable output.

The **Noise Margin** is therefore

$$NM = \min\{HNM, LNM\}$$

With the above five characteristics of a transistor, it is common to compare various families using the **Speed-Power Product**. This is the product of the propagation delay and the Power dissipated by an IC.