EEE 3131 ASSIGNMENT THREE (APRIL 2021)

Due: 24/05/2021

Question one

(a) State two disadvantages of Integrated Circuits (ICs)
(b) How many inputs of a low-power Schottky TTL NAND can be reliably driven from a single output of a Schottky TTL NAND, given the following relevant specifications for the devices of two TTLsubfamilies:

Schottky TTL: I_{OH}=1.0 mA; I_{IH}= 0.05 mA; I_{OL}=20.0 mA; I_{IL}=2.0mA

Low-power Schottky TTL: I_{OH}=0.4 mA; I_{IH}= 0.02 mA; I_{OL}=8.0 mA; I_{IL}=0.4mA

Question two

Explain and simulate using multisim the working principles of the following (for the simulation, only submit screenshots of the circuits):

(a) Diode Transitor Logic (DTL), NAND gate
(b) Resistor Transitor Logic (RTL), NOR gate

Question three

Draw/show the diagram of a schottky transistor and explain its operation (screenshots of the diagram are welcome).

Question four

Explain the differences in the behavior of power dissipation vs frequency for TTL and CMOS circuits.

Question five

Explain the working principle of an OR/NOR gate implemented using ECL logic family.

Question six

(a) What IC specifications are used to determine how many gates of one family can be driven from the output of another family?
(b) List the names and abbreviations of the four input and output currents of a digital IC.
(c) What effect did the Schottky-clamped transistor have on the operation of the standard TTL IC?

Question seven

(a) What does the negative sign in the rating of source current (e.g.,*IOH* __400 μA) signify?
(b) For TTL outputs, which is higher, the source current or the sink current?
(c) Which type of transistor, bipolar or field effect, is used in TTL ICs? In CMOS ICs?
(d) What is the principal reason that ECL ICs reach such high switching speeds?

Question eight

The input and output waveforms to an OR gate are given in Figure 3.1 Determine:
(a) The period and frequency of *V*in
(b) The rise and fall times (*tr*, *tf*) of *V*in
(c) The propagation delay times of (*tPLH*, *tPHL*) of the OR gate

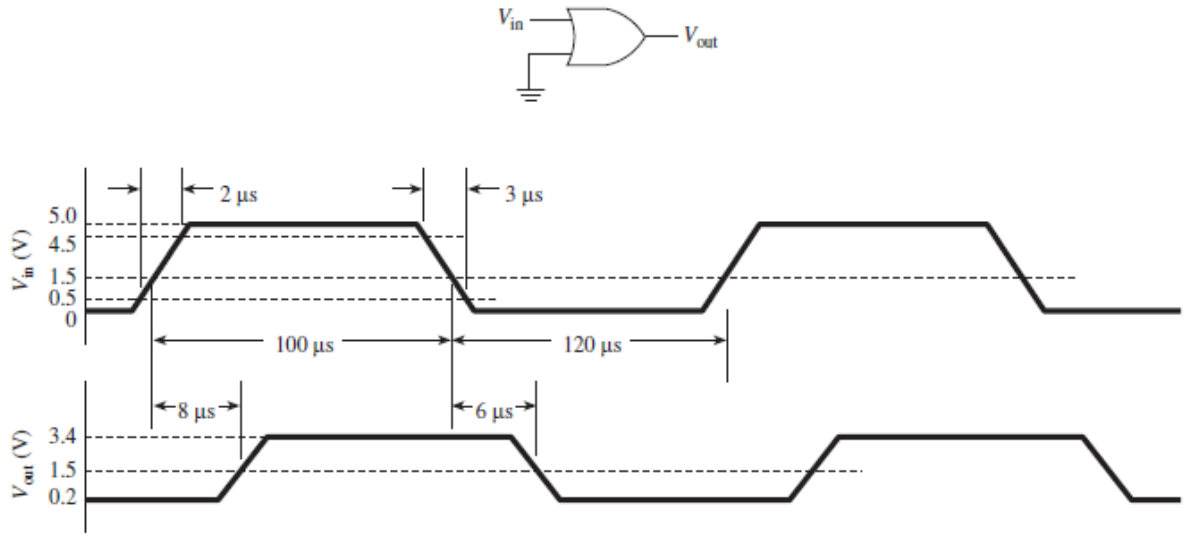

Figure 3.1

Question nine

(a) Find *Va* and *Ia* for Figure 3.2

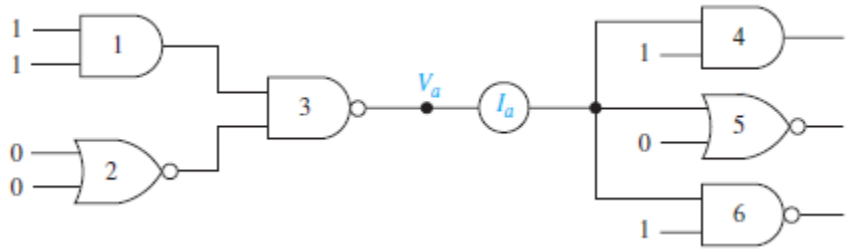

Figure 3.2

Question 10

Briefly describe **propagation delay**, **power dissipation**, **speed–power product**, **fan-out** and **noise margin** parameters.