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# EEE3571 Electronic Engineering I

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## Lecture 6: Field Effect Transistors



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# References

Our main reference text books in this course are

- [1] Neil S., [Electronics: A Systems Approach](#), 4th edition, 2009, Pearson Education Limited, ISBN 978-0-273-71918-2.
- [2] Boylestad R. L., Nashelsky L., [Electronic Devices and Circuit Theory](#), 11<sup>th</sup> Ed, 2013, Prentice-Hall, ISBN 978-0-13-262226-4.
- [3] Smith R. J., Dorf R. C., [Circuits Devices and Systems](#), 5<sup>th</sup> Ed., 2004, John Wiley, ISBN ISBN 9971-51-172-X.

However, feel free to use pretty much any additional text which you might find relevant to our course.

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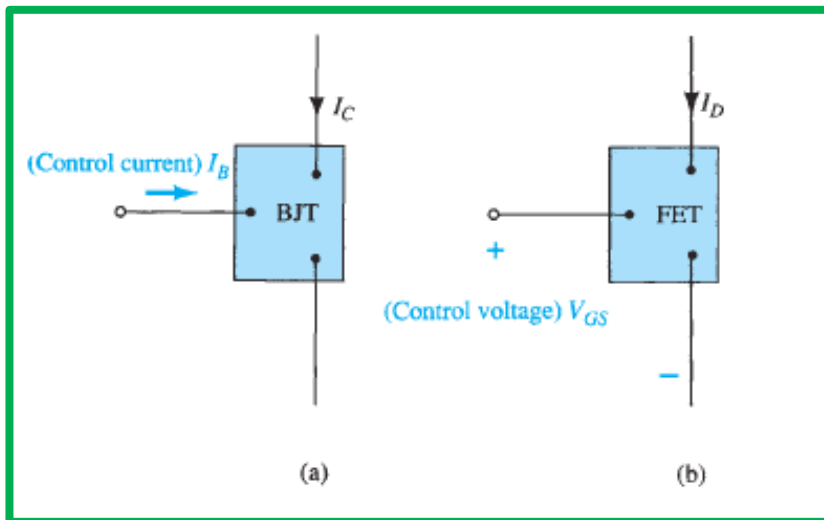
# Learning Objectives

At the end of the lecture 6 on [Field Effect Transistors](#), you ought to:

- 1) Become familiar with the construction and operating characteristics of Junction Field Effect (JFET), Metal-Oxide Semiconductor FET (MOSFET). Metal-Semiconductor FET (MESFET) transistors will not be covered.
- 2) Be able to sketch the transfer characteristics from the drain characteristics of a JFET and MOSFET transistor.
- 3) Understand the key parameters provided on the specification sheet for each type of FET.
- 4) Be aware of the differences between the dc analysis of the various types of FETs.

# 6.1 Introduction

- ❑ The Field Effect Transistor (FET) is a three-terminal device used for a wide range of applications, similar to those for BJTs.
- ❑ The primary difference between FETs and BJTs is the fact that: the BJT is a current-controlled device as depicted in Fig. 6.1a, whereas the JFET is a voltage-controlled device as shown in Fig. 6.1b.



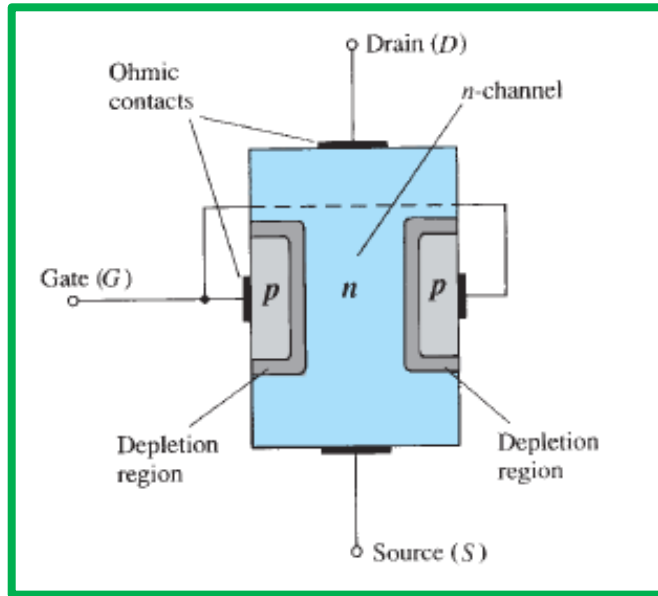
**Figure 6.1:** (a) Current-controlled; (b) voltage-controlled amplifiers.

- ❑ Just as there are *nnp* and *npn* BJTs, there *n-channel* and *p-channel* FETs.
- ❑ It is worth noting that while BJTs are bipolar, FETs are unipolar, as they depend wholly on either electron (*n-channel*) or hole (*p-channel*) condition.
- ❑ For FETs the electric field is established by charges present, which controls the conduction path of the output circuit.

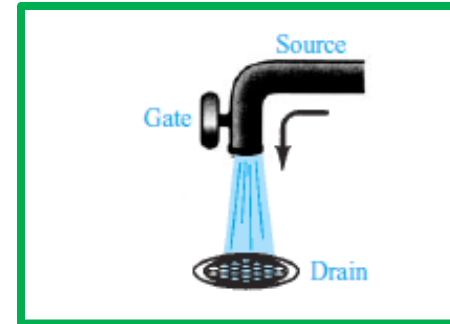
## 6.1 Introduction Cont'd

- ❑ One of the most important characteristics of the FET is its high input impedance.
- ❑ This is a critical characteristic in the design of linear ac amplifiers.
- ❑ Quiet on the contrary, typical ac voltage gain for BJT amplifiers are a great deal more than for FETs.
- ❑ However, FETs are more temperature stable than BJTs, and FETs are usually smaller than BJTs, making them particularly useful in integrated-circuit (IC) chips
- ❑ 2 types to be discussed are: the junction field-effect transistor (JFET), the metal-oxide-semiconductor field effect transistor (MOSFET). Not included and the metal-semiconductor field effect transistor (MESFET).

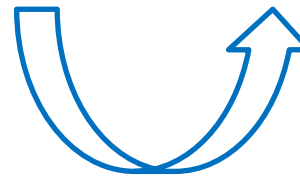
## 6.2 Construction and Characteristics of FETs



**Figure 6.2:** Junction field-effect transistor (JFET).



**Figure 6.3:** Water analogy for the JFET control mechanism.

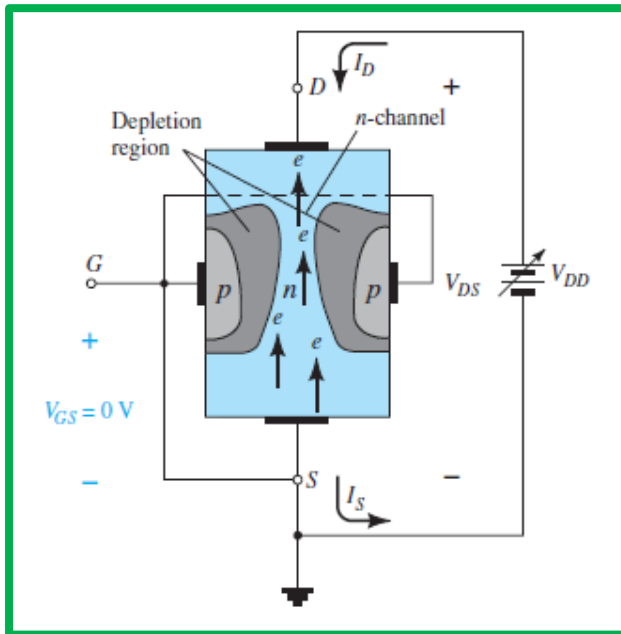


- ❑ For the JFET the *n-channel* device will be prominently discussed.
- ❑ For the JFET the *n-channel* device will be prominently discussed.
- ❑ In the absence of applied potentials the JFET has two *p-n junctions* under no bias

## 6.2 Construction and Characteristics of FETs

$V_{GS} = 0 \text{ V}$ ,  $V_{DS}$  Some Positive Value

□ In Fig. 6.4, a positive voltage  $V$  is applied across the channel and the gate is connected directly to the source to establish the condition  $V_{GS} = 0 \text{ V}$ .

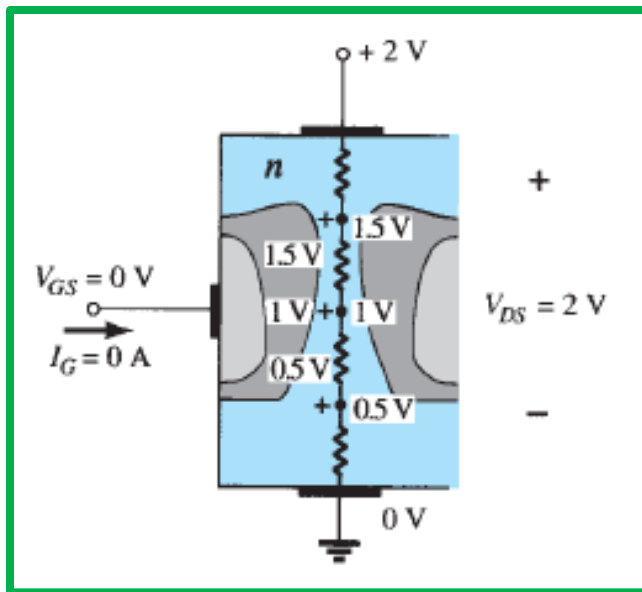


- Notice that as the voltage  $V_{DD} (= V_{DS})$  is applied, the electrons are drawn to the drain terminal, establishing the conventional current  $I_D$ .
- The path of charge flow shows that  $I_D = I_S$ .

**Figure 6.4:** JFET at  $V_{GS} = 0 \text{ V}$  and  $V_{DS} > 0 \text{ V}$ .

## 6.2 Construction and Characteristics of FETs Cont'd

- The depletion region is wider near the top of both  $p$ -type materials.
- Assuming a uniform resistance in the  $n$ -channel, we can break it down into divisions depicted in Fig. 6.5. Thus,  $I_D$  establishes voltage drops indicated.



- Notice that the upper region of the  $p$ -type material will be reverse-biased by about  $1.5\text{ V}$ , with the lower region only reverse-biased by  $0.5\text{ V}$ .
- Recall that the greater the applied reverse bias, the wider is the depletion region.
- An important characteristic of the JFET is that  $I_G = 0\text{ A}$ .

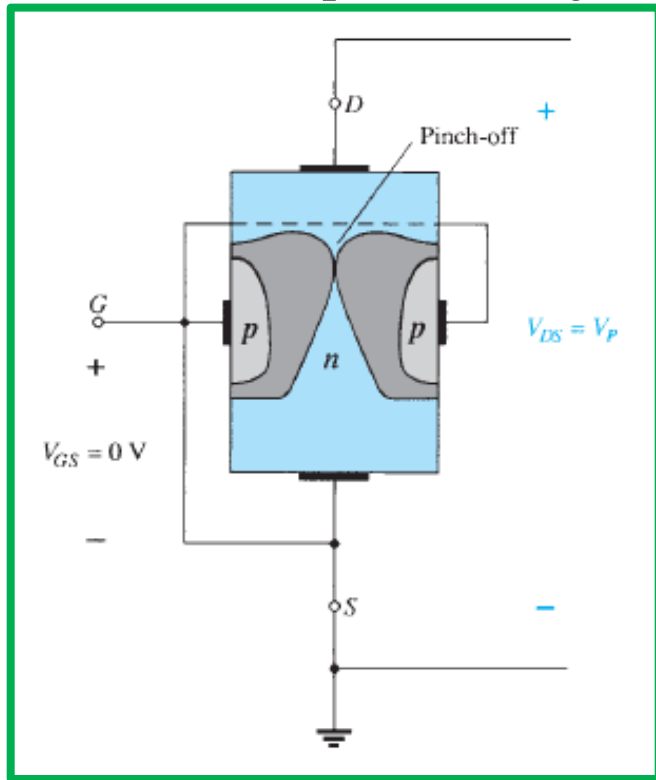
**Figure 6.5:** Varying reverse-bias potentials across the  $p$ - $n$  junction of an  $n$ -channel JFET.

## 6.2 Construction and Characteristics of FETs Cont'd

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## 6.2 Construction and Characteristics of FETs Cont'd

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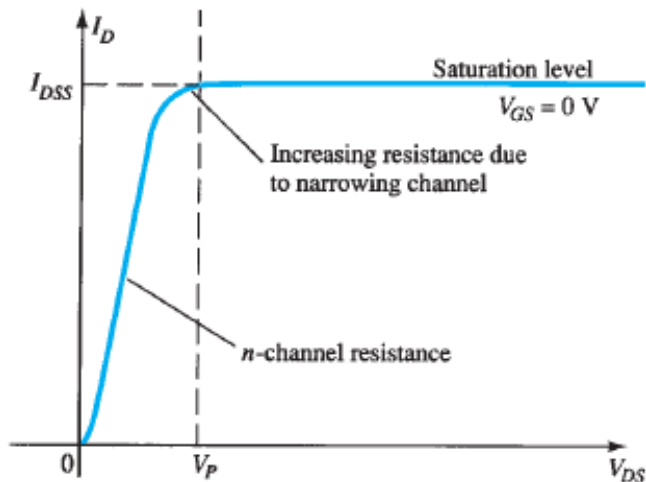


**Figure 6.7:** Pinch-off ( $V_{GS} = 0 \text{ V}$ ,  $V_{DS} = V_P$ ).

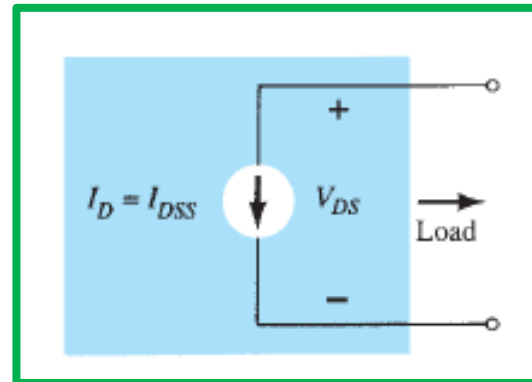
- ❑ Notice that the upper region of the  $p$ -type material will be reverse-biased by about  $1.5 \text{ V}$ , with the lower region only reverse-biased by  $0.5 \text{ V}$ .
- ❑ Recall that the greater the applied reverse bias, the wider is the depletion region.
- ❑ An **important characteristic** of the JFET is that  $I_G = 0 \text{ A}$ .

## 6.2 Construction and Characteristics of FETs Cont'd

- Beyond the pinch-off voltage,  $I_D$  maintains a saturation level as  $I_{DSS}$  in Fig. 6.6.
- In essence, once  $V_{DS} > V_p$  the JFET has the characteristics of a current source.
- Thus,  $I_{DSS}$  is the maximum drain current for a JFET and is defined by conditions  $V_{GS} = 0\text{ V}$  and  $V_{DS} > |V_p|$ .

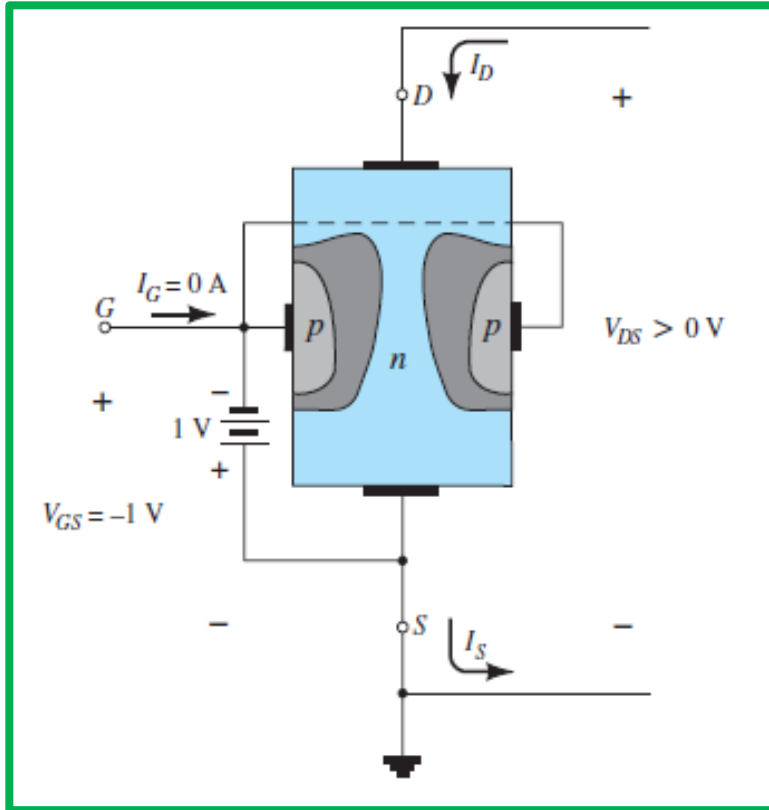


**Figure 6.6:**  $I_D$  versus  $V_{DS}$  for  $V_{GS} = 0\text{ V}$ .



**Figure 6.8:** current source equivalent for  $V_{GS} = 0\text{ V}$ ,  $V_{DS} > V_p$ .

## 6.2 Construction and Characteristics of FETs Cont'd

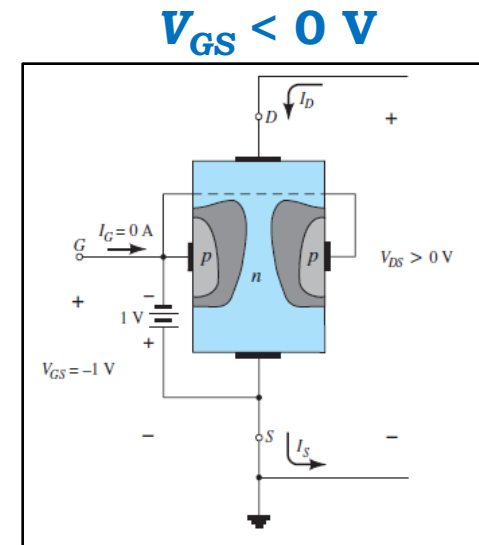
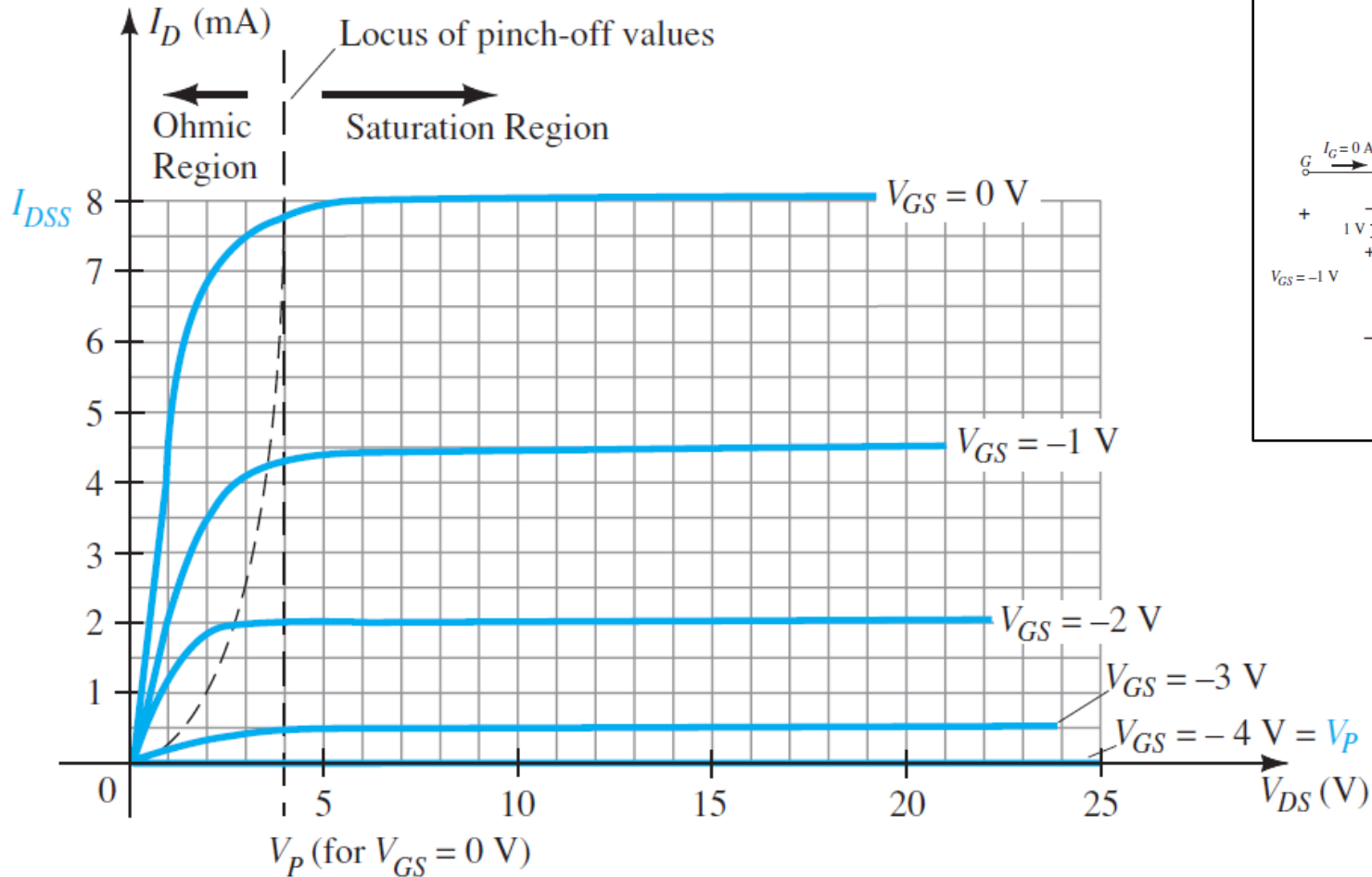


**Figure 6.9:** Application of a negative voltage to the gate of a JFET.

$$V_{GS} < 0\text{ V}$$

- Here, various curves of  $I_D$  versus  $V_{DS}$  for various levels of  $V_{GS}$  can be developed for the JFET.
- The level of  $V_{GS}$  that results in  $I_D = 0\text{ mA}$  is defined by  $V_{GS} = V_p$ , with  $V_p$  being a negative for  $n$ -channel devices and a positive voltage for  $p$ -channel JFETs.
- On most specification sheets the pinch-off voltage is specified as  $V_{GS(off)}$  rather than  $V_p$ .

# 6.2 Construction and Characteristics of FETs Cont'd



**FIG. 6.11**

*n*-Channel JFET characteristics with  $I_{DSS} = 8$  mA and  $V_P = -4$  V.

## 6.2 Construction and Characteristics of FETs Cont'd

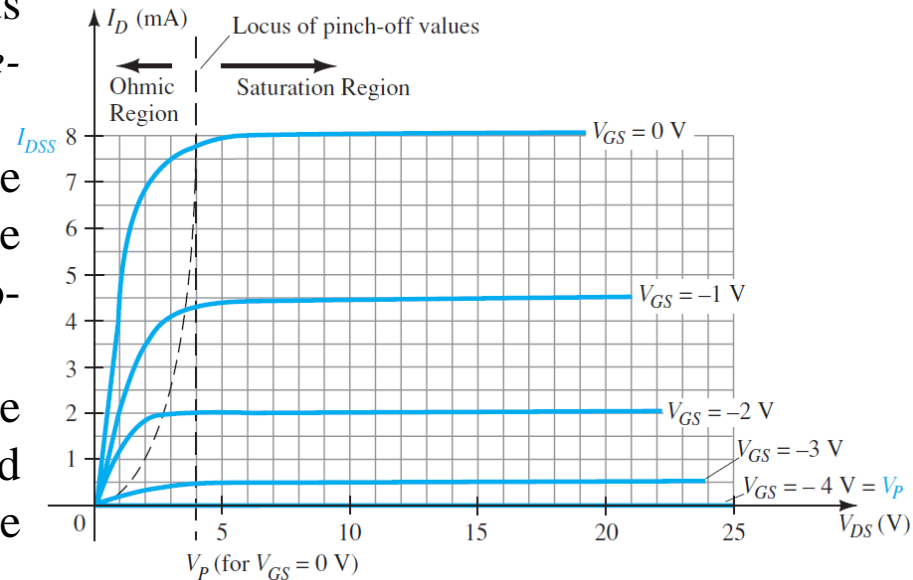
□ The region to the left of the pinch-off locus is referred to as the *ohmic or voltage-controlled resistance* region.

□ In this region the JFET can actually be employed as a variable resistor; whose resistance is controlled by the applied gate-to-source voltage.

□ Note the slope of each curve and therefore the resistance of the device between drain and source for  $V_{DS} < V_P$  are a function of the applied voltage  $V_{GS}$ .

□ As  $V_{GS}$  becomes more and more negative, the slope of each curve becomes more and more horizontal, corresponding to an increasing resistance level.

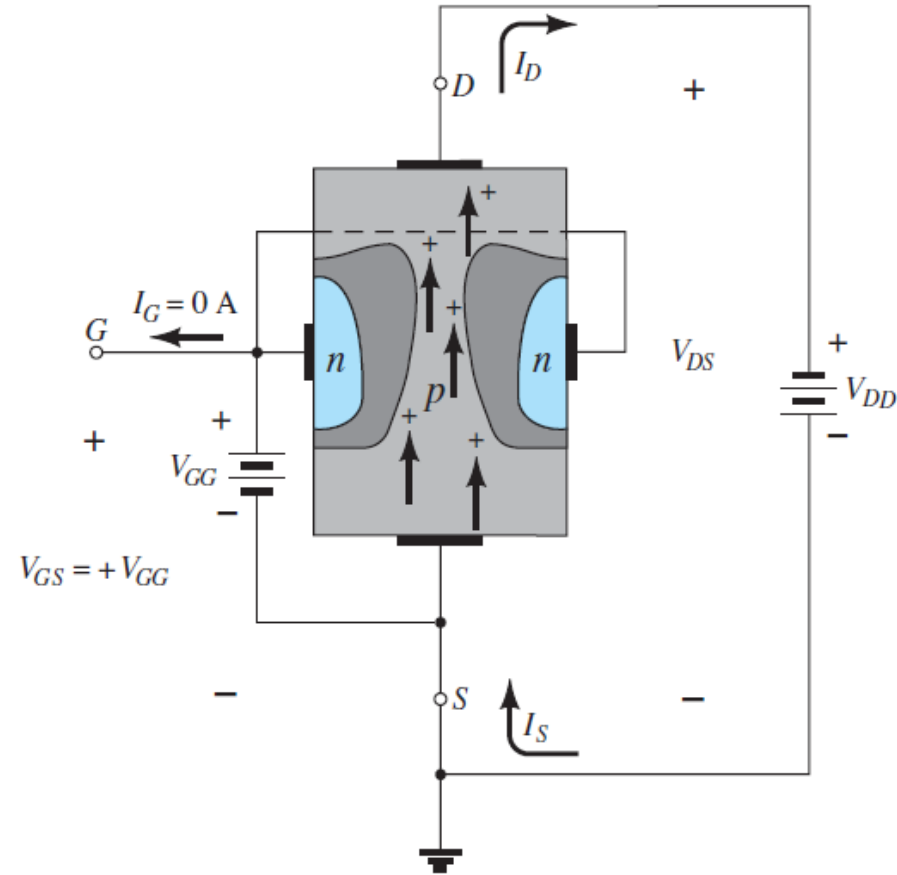
□ The following equation provides a good first approximation to the resistance level in terms of the applied voltage  $V_{GS}$ :



$$r_d = \frac{r_o}{(1 - V_{GS}/V_P)^2}$$

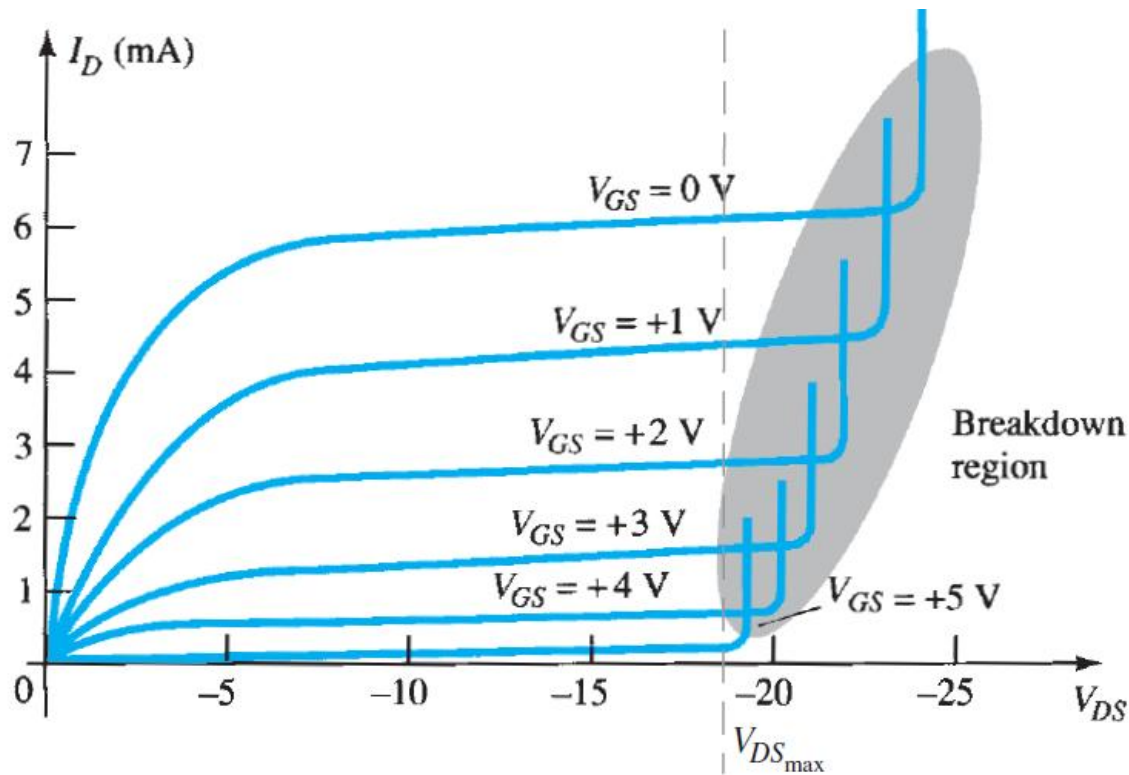
# Construction of P-Channel JFET

- ❑ The p -channel JFET is constructed in exactly the same manner as the n -channel device of but with a reversal of the p - and n -type materials
- ❑ The defined current directions are reversed, as are the actual polarities for the voltages  $V_{GS}$  and  $V_{DS}$ .
- ❑ For the p -channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for  $V_{DS}$  will result in negative voltages for  $V_{DS}$  on the characteristics.



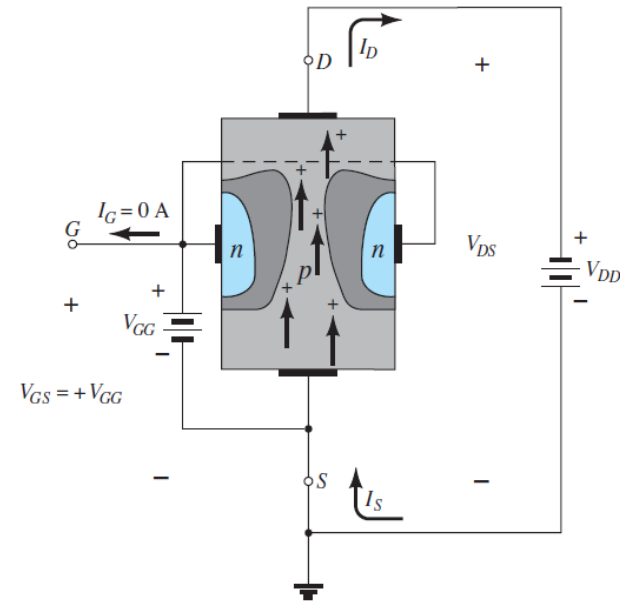
**FIG. 6.12**  
*p-Channel JFET.*

# Construction of P-Channel JFET



**FIG. 6.13**

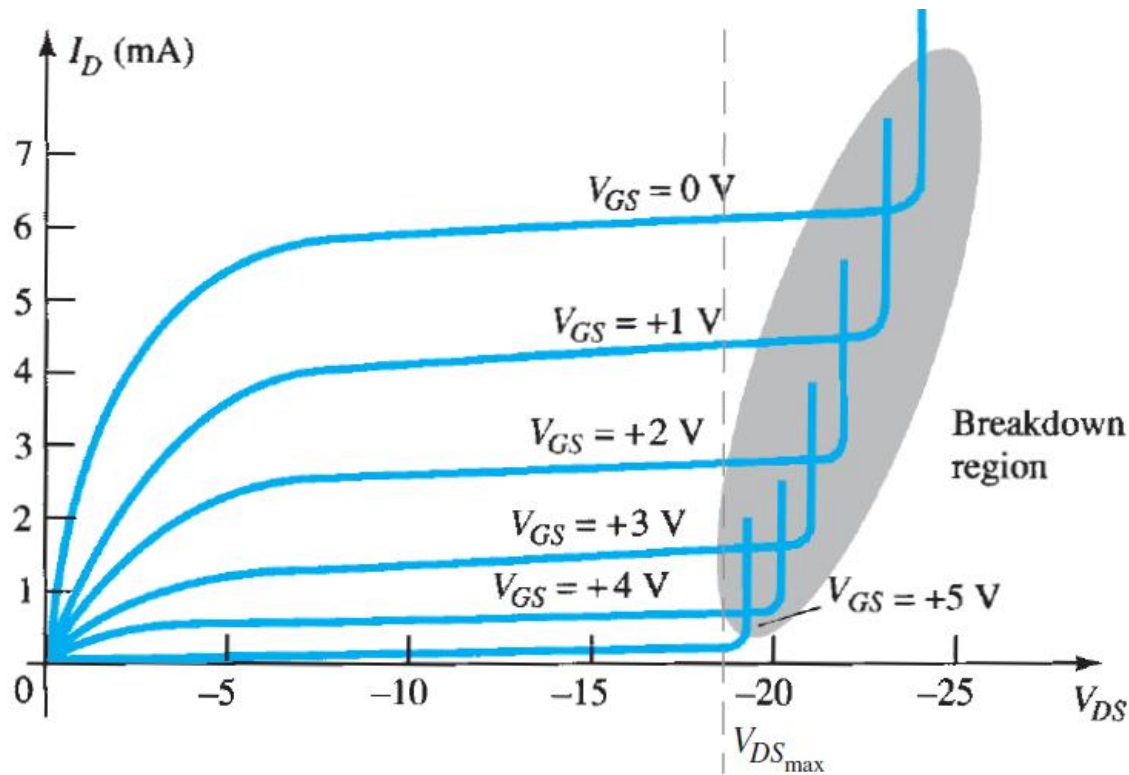
*p*-Channel JFET characteristics with  $I_{DSS} = 6 \text{ mA}$  and  $V_P = +6 \text{ V}$ .



**FIG. 6.12**  
*p*-Channel JFET.

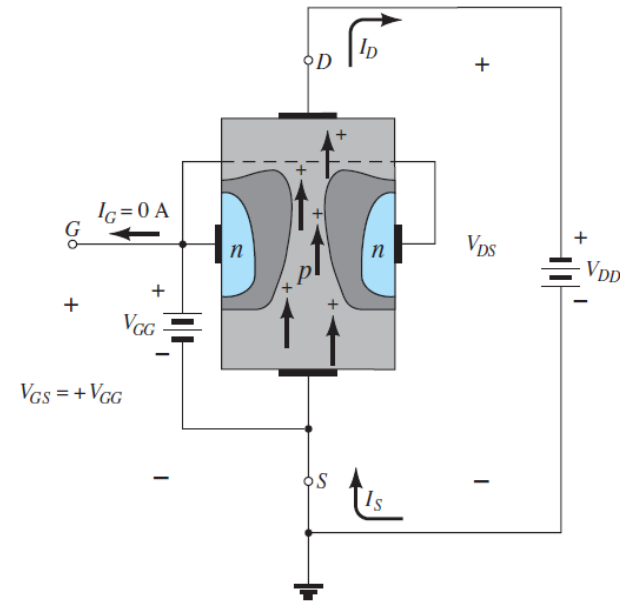
- ❑ At high levels of  $V_{DS}$  the curves suddenly rise to levels that seem unbounded.
- ❑ This vertical rise is an indication that breakdown has occurred and the current through the channel is now limited solely by the external circuit.
- ❑ This also occurs for the n -channel device if sufficient voltage is applied.
- ❑ This region can be avoided if the level of  $V_{DSmax}$  is noted on the specification sheet and the design is such that  $V_{DS} < V_{DSmax}$  for all values of  $V_{GS}$ .

# Construction of P-Channel JFET



**FIG. 6.13**

*p*-Channel JFET characteristics with  $I_{DSS} = 6$  mA and  $V_P = +6$  V.

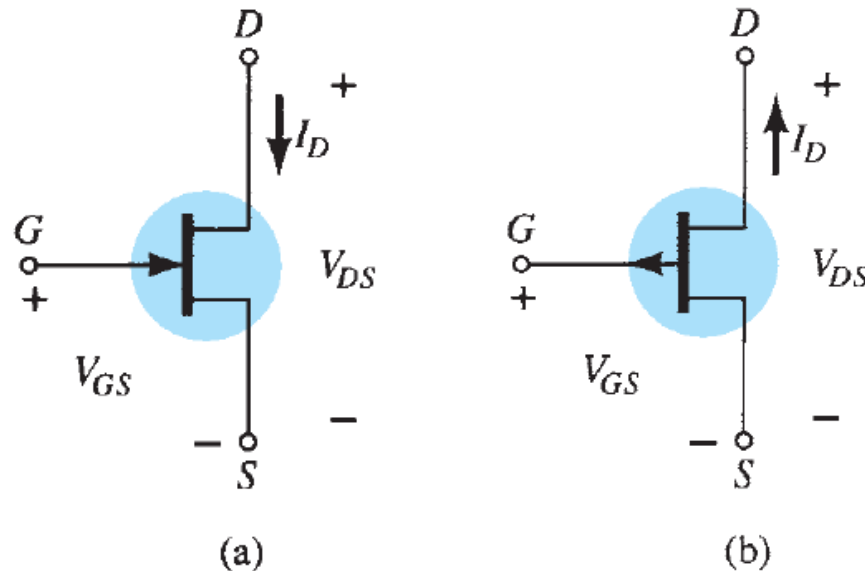


**FIG. 6.12**  
*p*-Channel JFET.

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- ❑ This also occurs for the n -channel device if sufficient voltage is applied.
- ❑ This region can be avoided if the level of  $V_{DS_{max}}$  is noted on the specification sheet and the design is such that  $V_{DS} < V_{DS_{max}}$  for all values of  $V_{GS}$ .

# JFET Symbols

- ❑ The arrow is pointing in for the  $n$ -channel device of Fig. 6.14a to represent the direction in which  $I_G$  would flow if the  $p$ - $n$  junction were forward-biased.
- ❑ For the  $p$ -channel device the only difference in the symbol is the direction of the arrow in the symbol.



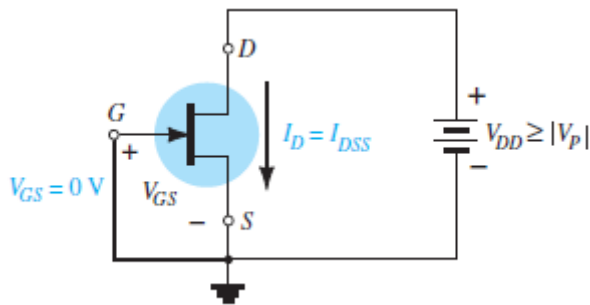
**FIG. 6.14**

*JFET symbols: (a)  $n$ -channel; (b)  $p$ -channel.*

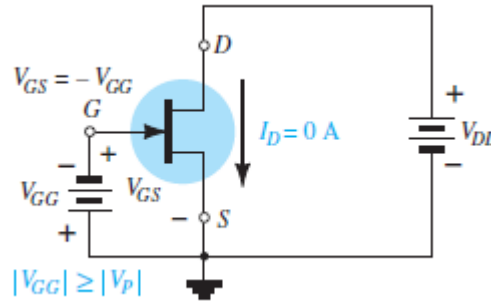
# Summary of JFET Characteristics

## n-Channel JFET:

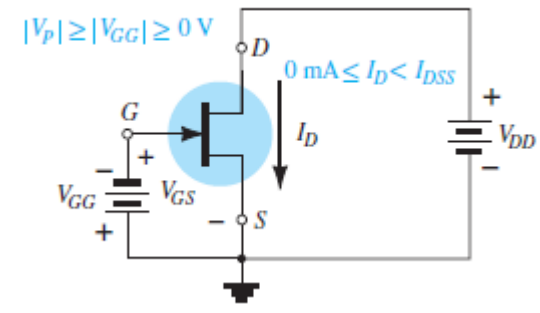
- The maximum current is defined as  $I_{DSS}$  and occurs when  $V_{GS} = 0\text{ V}$  and  $V_{DS} \geq V_P$ .
  - For gate-to-source voltages  $V_{GS} < V_P$  (or more negative than the pinch-off level), the drain current  $I_D = 0\text{ A}$ .
  - For all levels of  $V_P < V_{GS} < 0\text{ V}$ ,  $I_D$  will range between  $I_{DSS}$  and  $0\text{ A}$ .
- A similar list can be developed for p-channel JFETs.



a)



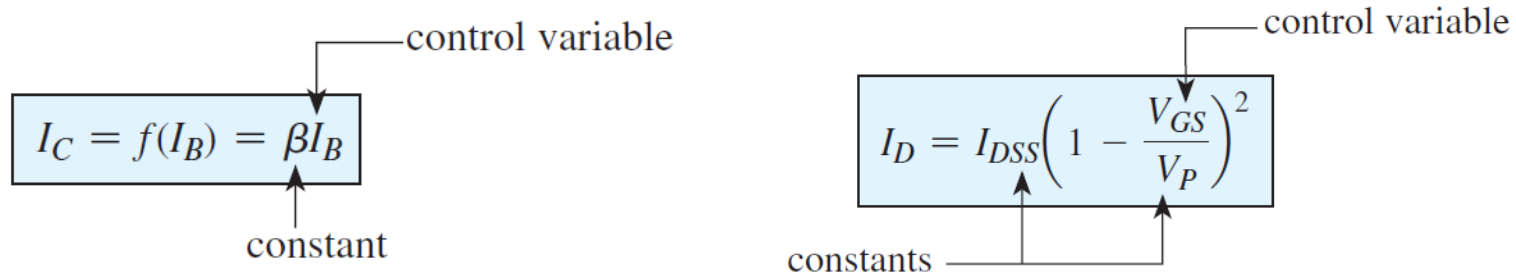
b)



c)

# JFET Transfer Characteristics

- ❑ For the BJT transistor the output current  $I_C$  and the input controlling current  $I_B$  are related by beta, which was considered constant for the analysis to be performed.
- ❑ The relationship between  $I_D$  and  $V_{GS}$  is defined by Shockley's equation.



- ❑ For the dc analysis to be performed a graphical rather than a mathematical approach will in general be more direct and easier to apply.
- ❑ The graphical approach, however, will require a plot of Shockley's equation to represent the device and a plot of the network equation relating the same variables.
  - The solution is defined by the point of intersection of the two curves.
- ❑ It is important to keep in mind when applying the graphical approach that the device characteristics will be unaffected by the network in which the device is employed.

# JFET Transfer Characteristics

- Since the transfer curve must be plotted so frequently, a shorthand method for plotting the curve quickly, efficiently and with acceptable degree of accuracy is used:

$$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$$

control variable

constants

**TABLE 6.1**

*V<sub>GS</sub> versus I<sub>D</sub> Using Shockley's Equation*

<b>V<sub>GS</sub></b>	<b>I<sub>D</sub></b>
0	<i>I<sub>DSS</sub></i>
0.3 <i>V<sub>P</sub></i>	<i>I<sub>DSS</sub>/2</i>
0.5 <i>V<sub>P</sub></i>	<i>I<sub>DSS</sub>/4</i>
<i>V<sub>P</sub></i>	0 mA

# JFET Transfer Characteristics

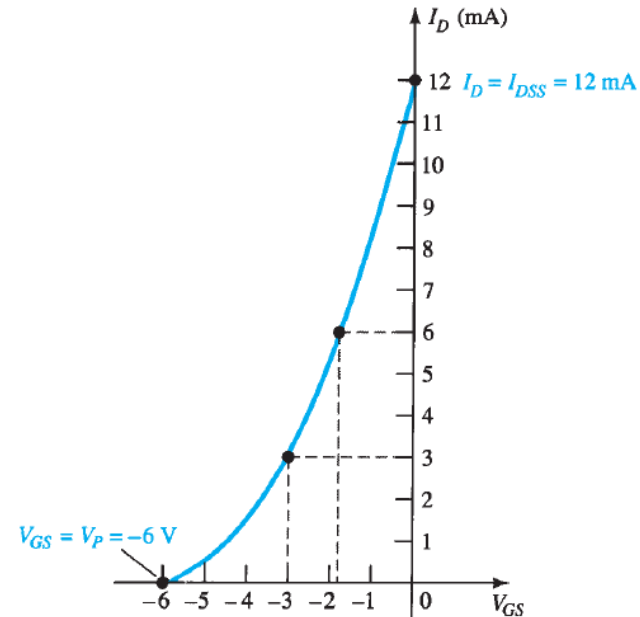
**EXAMPLE 6.1** Sketch the transfer curve defined by  $I_{DSS} = 12 \text{ mA}$  and  $V_P = -6 \text{ V}$ .

**Solution:** Two plot points are defined by

$$I_{DSS} = 12 \text{ mA} \quad \text{and} \quad V_{GS} = 0 \text{ V}$$

and  $I_D = 0 \text{ mA}$  and  $V_{GS} = V_P$

At  $V_{GS} = V_P/2 = -6 \text{ V}/2 = -3 \text{ V}$  the drain current is determined by  $I_D = I_{DSS}/4 = 12 \text{ mA}/4 = 3 \text{ mA}$ . At  $I_D = I_{DSS}/2 = 12 \text{ mA}/2 = 6 \text{ mA}$  the gate-to-source voltage is determined by  $V_{GS} \cong 0.3V_P = 0.3(-6 \text{ V}) = -1.8 \text{ V}$ . All four plot points are well defined on Fig. 6.18 with the complete transfer curve.



**FIG. 6.18**

Transfer curve for Example 6.1.

# JFET Specification Sheet

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
$V_{DS}$	Drain-Source Voltage	25	V
$V_{DG}$	Drain-Gate Voltage	25	V
$V_{GS}$	Gate-Source Voltage	-25	V
$I_{GF}$	Forward Gate Current	10	mA
$T_j, T_{stg}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

## THERMAL CHARACTERISTICS

Symbol	Characteristic	Max		Units
		2N5457	*MMBF5457	
$P_D$	Total Device Dissipation Derate above 25°C	625	350	mW
		5.0	2.8	mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	556	°C/W

## ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise noted

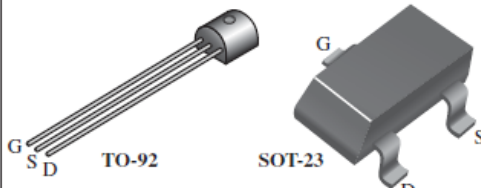
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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## OFF CHARACTERISTICS

$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	$I_G = 10 \mu\text{A}, V_{DS} = 0$	-25			V
$I_{GSS}$	Gate Reverse Current	$V_{GS} = -15 \text{ V}, V_{DS} = 0$			-1.0	nA
		$V_{GS} = -15 \text{ V}, V_{DS} = 0, T_A = 100^\circ\text{C}$			-200	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15 \text{ V}, I_D = 10 \text{ nA}$	5457	-0.5	-6.0	V
$V_{GS}$	Gate-Source Voltage	$V_{DS} = 15 \text{ V}, I_D = 100 \mu\text{A}$	5457	-2.5		V

**FAIRCHILD**  
SEMICONDUCTOR™

**2N5457**      **MMBF5457**



TO-92      SOT-23

NOTE: Source & Drain are interchangeable

**N-Channel General Purpose Amplifier**  
This device is a low-level audio amplifier and switching transistor, and can be used for analog switching applications.

# JFET Specification Sheet

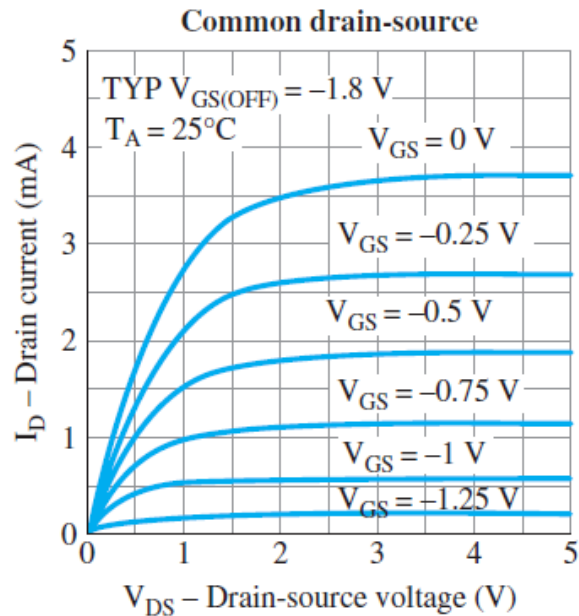
## ON CHARACTERISTICS

$I_{DSS}$	Zero-Gate Voltage Drain Current	$V_{DS} = 15 \text{ V}, V_{GS} = 0$	5457	1.0	3.0	5.0	mA
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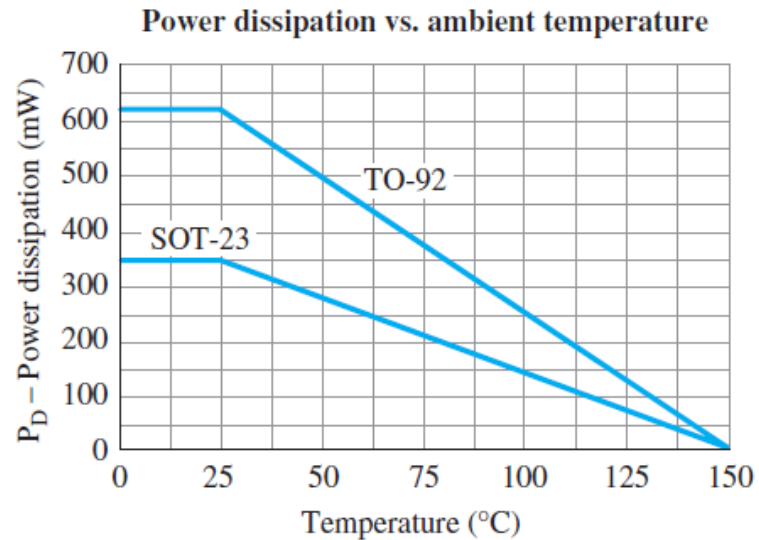
## SMALL SIGNAL CHARACTERISTICS

$g_{fs}$	Forward Transfer Conductance	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ kHz}$	5457	1000		5000	$\mu\text{mhos}$
$g_{os}$	Output Conductance	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$			10	50	$\mu\text{mhos}$
$C_{iss}$	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$			4.5	7.0	pF
$C_{rss}$	Reverse Transfer Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$			1.5	3.0	pF
NF	Noise Figure	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ kHz},$ $R_G = 1.0 \text{ megohm}, BW = 1.0 \text{ Hz}$				3.0	dB

(a)

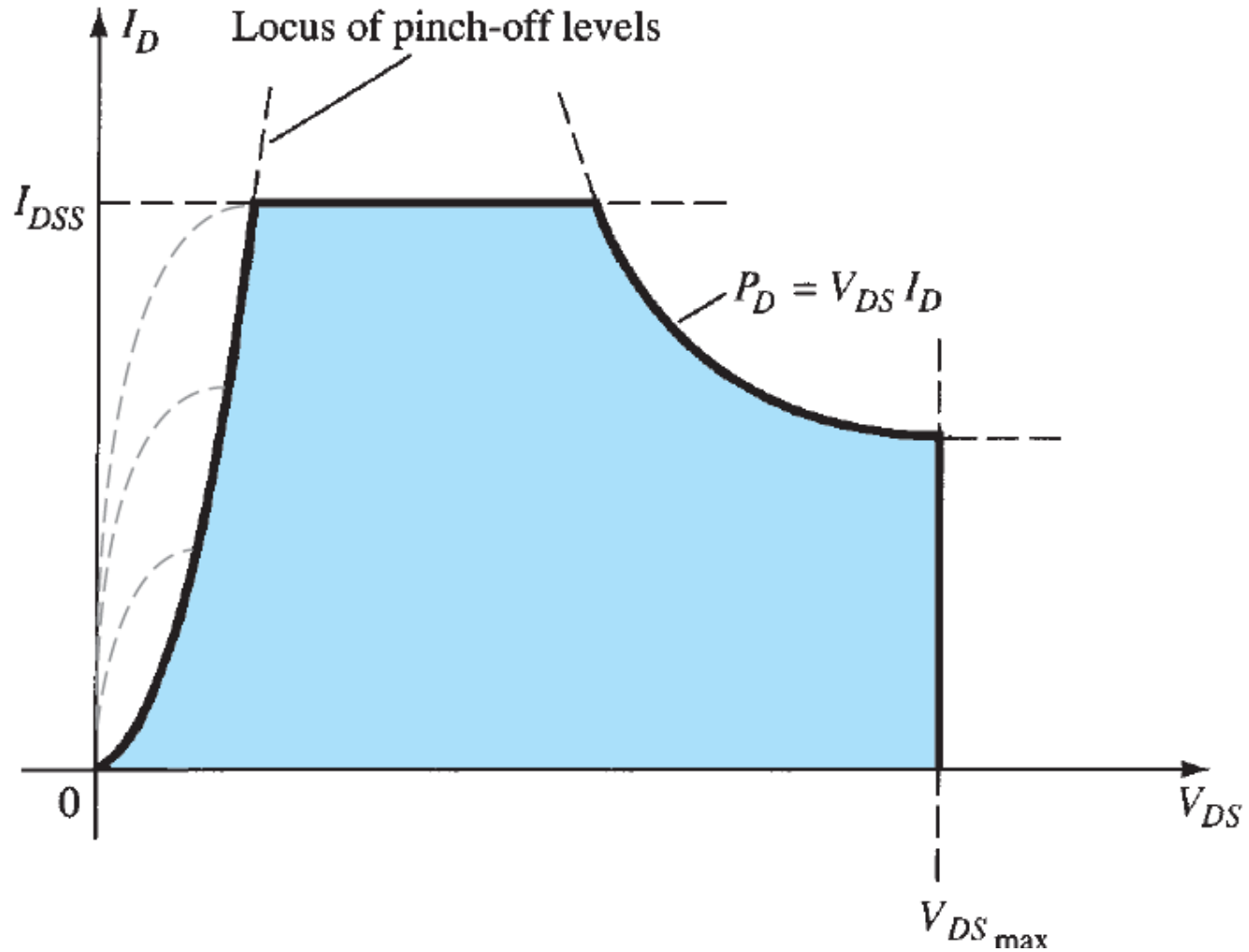


(b)



(c)

# JFET Operating Region



**FIG. 6.21**

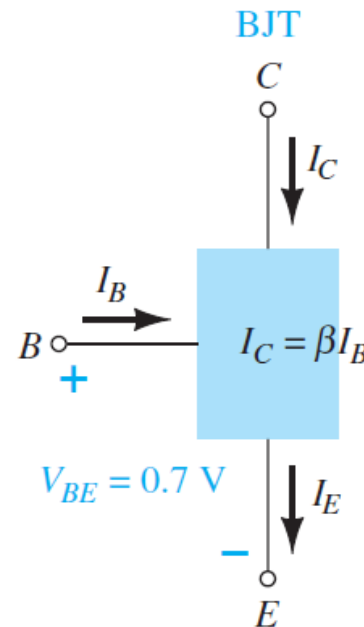
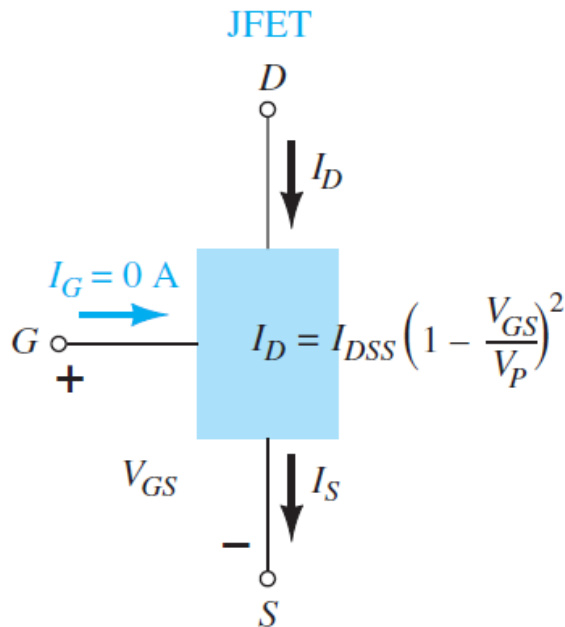
*Normal operating region for linear amplifier design.*

# JFET Specification Sheet

- The electrical characteristics include the level of  $V_P$  in the “off” characteristics,  $I_{DSS}$  in the “on” characteristics.
- $V_P = V_{GS(off)}$  has a range from -0.5 V to -6.0 V and
- $I_{DSS}$  from 1 mA to 5 mA.
- The fact that both will vary from device to device with the same nameplate identification must be considered in the design process.

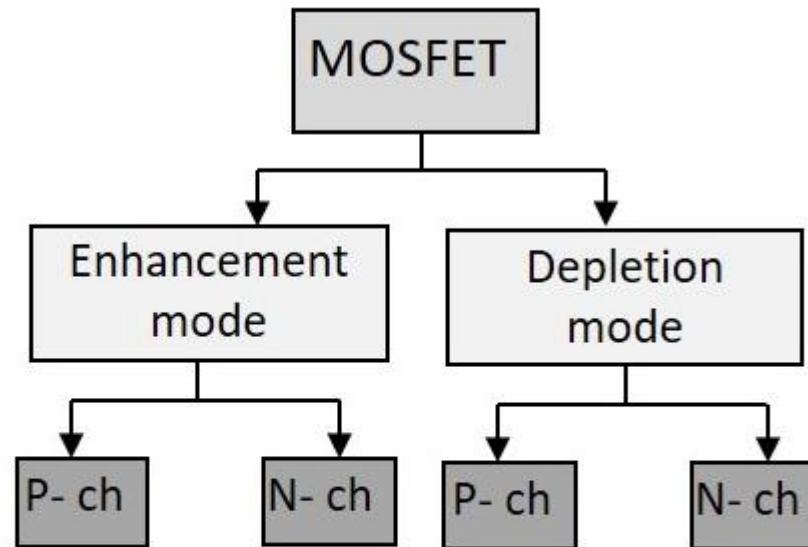
# Comparison of JFET with BJT

<i>JFET</i>	$\Leftrightarrow$	<i>BJT</i>
$I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2$		$I_C = \beta I_B$
$I_D = I_S$		$I_C \cong I_E$
$I_G \cong 0 \text{ A}$		$V_{BE} \cong 0.7 \text{ V}$



# Introduction to MOSFETS

- ❑ There are three types of FETs: JFETs, MOSFETs, and MESFETs.
- ❑ MOSFETs are further broken down into depletion type and enhancement type.

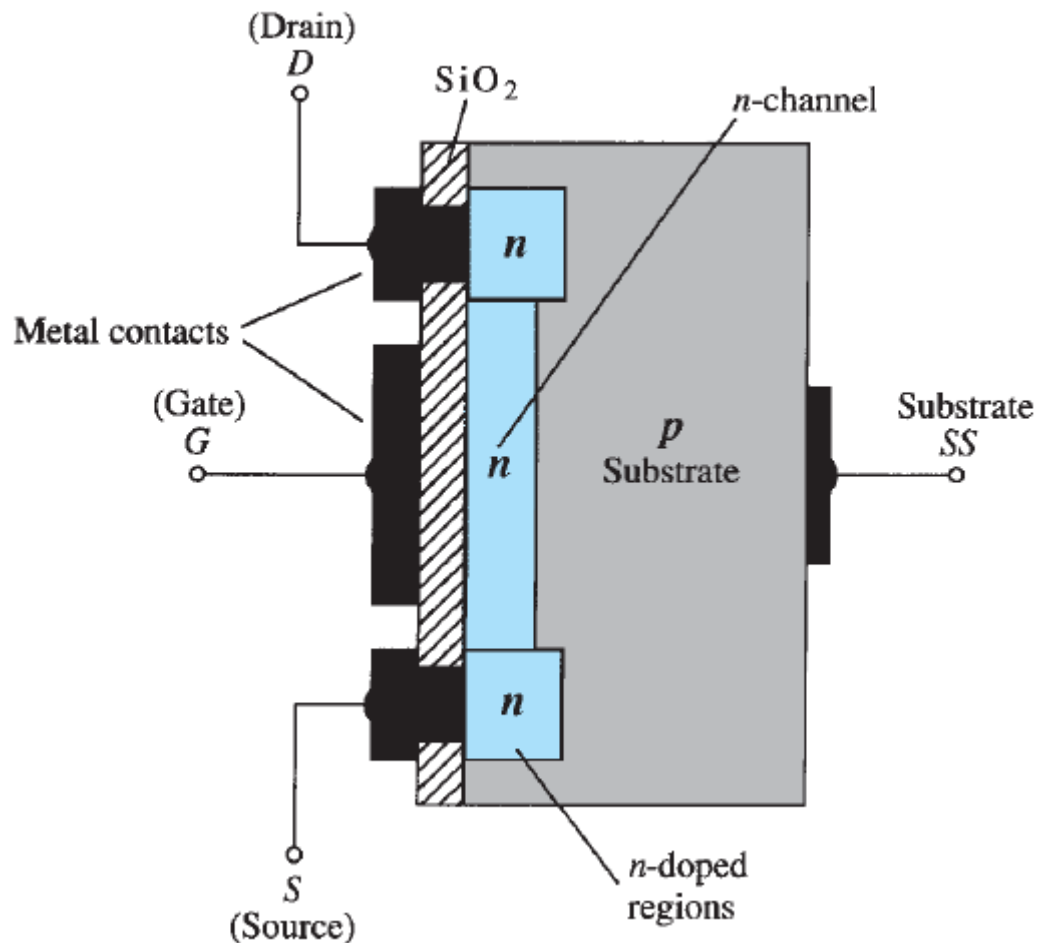


- P- ch = P- channel
- N- ch = N- channel

# Introduction to MOSFETS

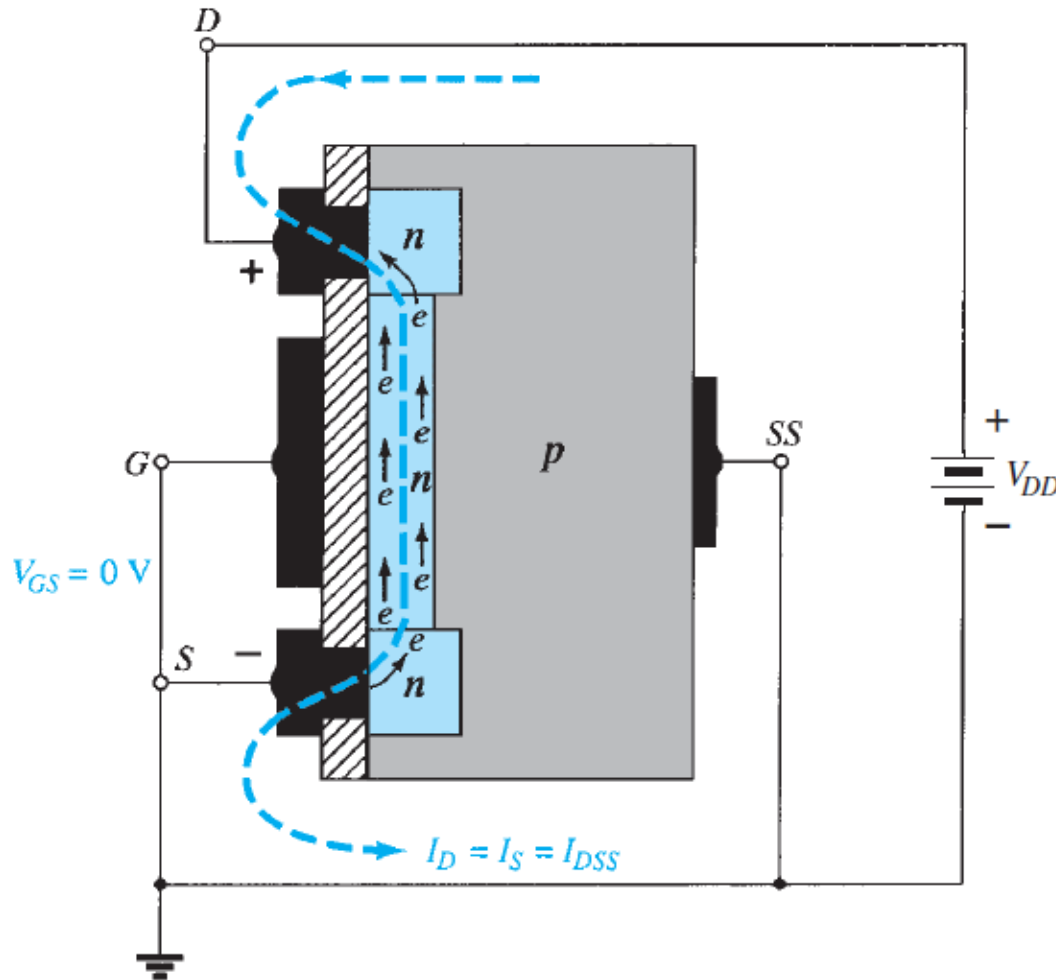
- ❑ The terms depletion and enhancement define their basic mode of operation.
- ❑ The name MOSFET stands for metal–oxide–semiconductor field-effect transistor (name will make more sense when studying structure).
- ❑ In this section we examine the depletion-type MOSFET, which has characteristics similar to those of a JFET between cutoff and saturation at  $I_{DSS}$  ,

# Structure of n-Channel Depletion-type MOSFETS



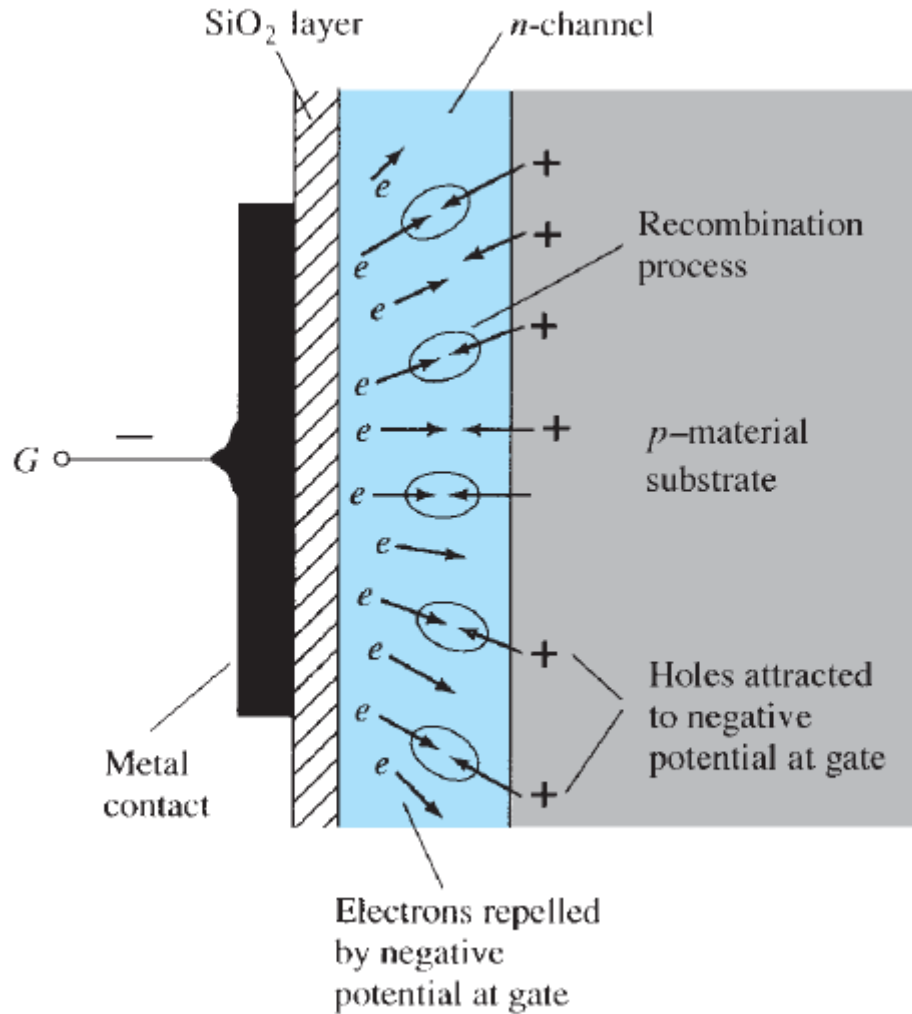
- ❑ A slab of p -type material is formed from a silicon base.
- ❑ In some cases the substrate is internally connected to the source terminal.
- ❑ The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel.
- ❑ The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin silicon dioxide (SiO<sub>2</sub>) layer.
- ❑ This accounts for the very desirable high input impedance of the device.
- ❑ The input resistance of a MOSFET is usually more than that of a typical JFET

# Basic Operation and Characteristics n-Channel Depletion-type MOSFETS



- Gate-to-source voltage is set to 0 V
- $V_{DD}$  is applied across the drain-to-source terminals.
- This results in an attraction of the free electrons of the n-channel for the positive voltage at the drain.
- Resulting in a current similar to that flowing in the channel of the JFET.
- In fact, the resulting current with  $V_{GS} = 0V$  continues to be labelled  $I_{DSS}$ .
- What will happen for  $V_{GS} < 0$  and  $V_{GS} > 0$ ?

# Basic Operation and Characteristics n-Channel Depletion-type MOSFETS



$$V_{GS} < 0$$

- The negative potential at the gate will tend to pressure electrons toward the p -type substrate (like charges repel) and attract holes from the p -type substrate
  - a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the n -channel available for conduction.

# Basic Operation and Characteristics

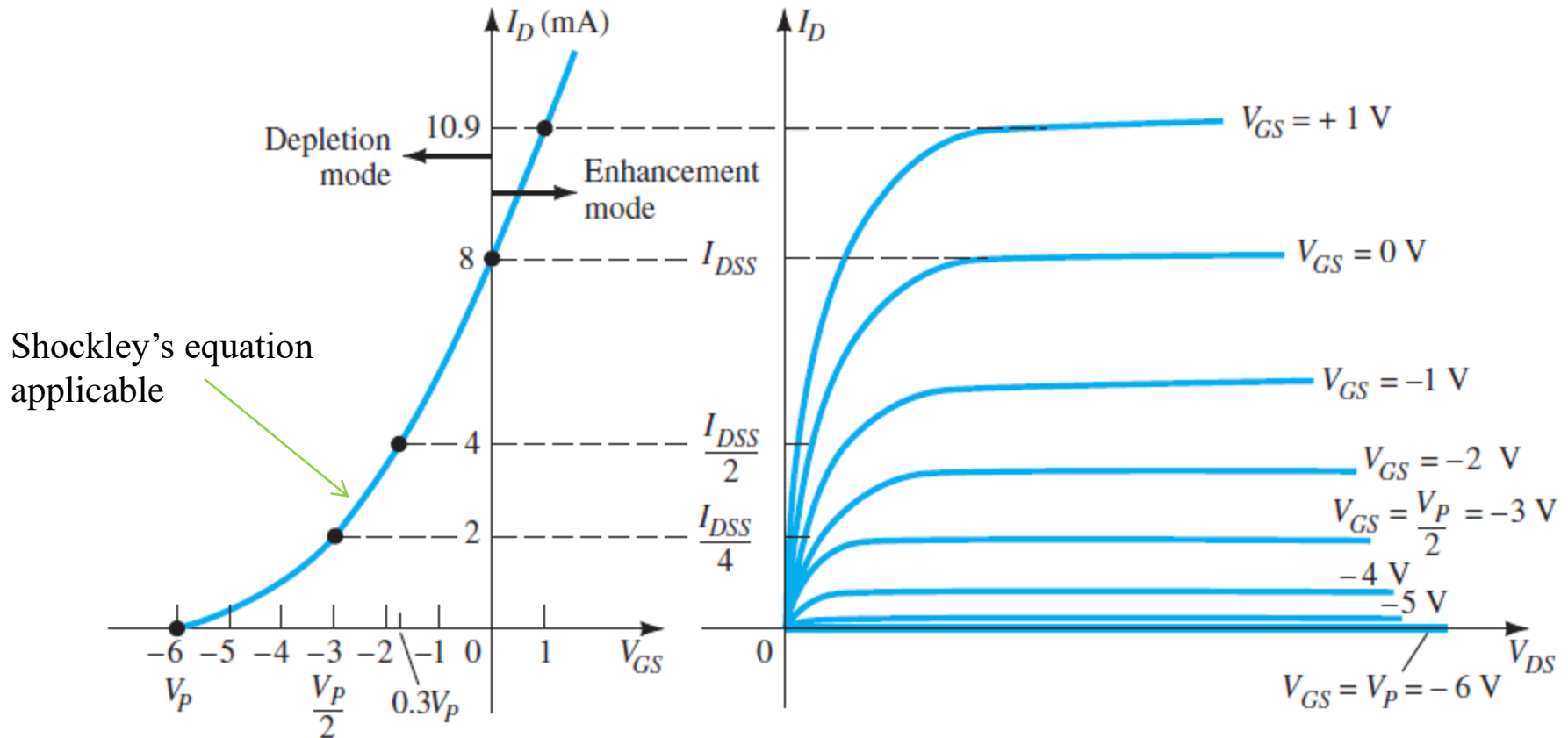
## n-Channel Depletion-type MOSFETS

$$V_{GS} > 0$$

- The positive gate will draw additional electrons (free carriers) from the  $p$ -type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles.

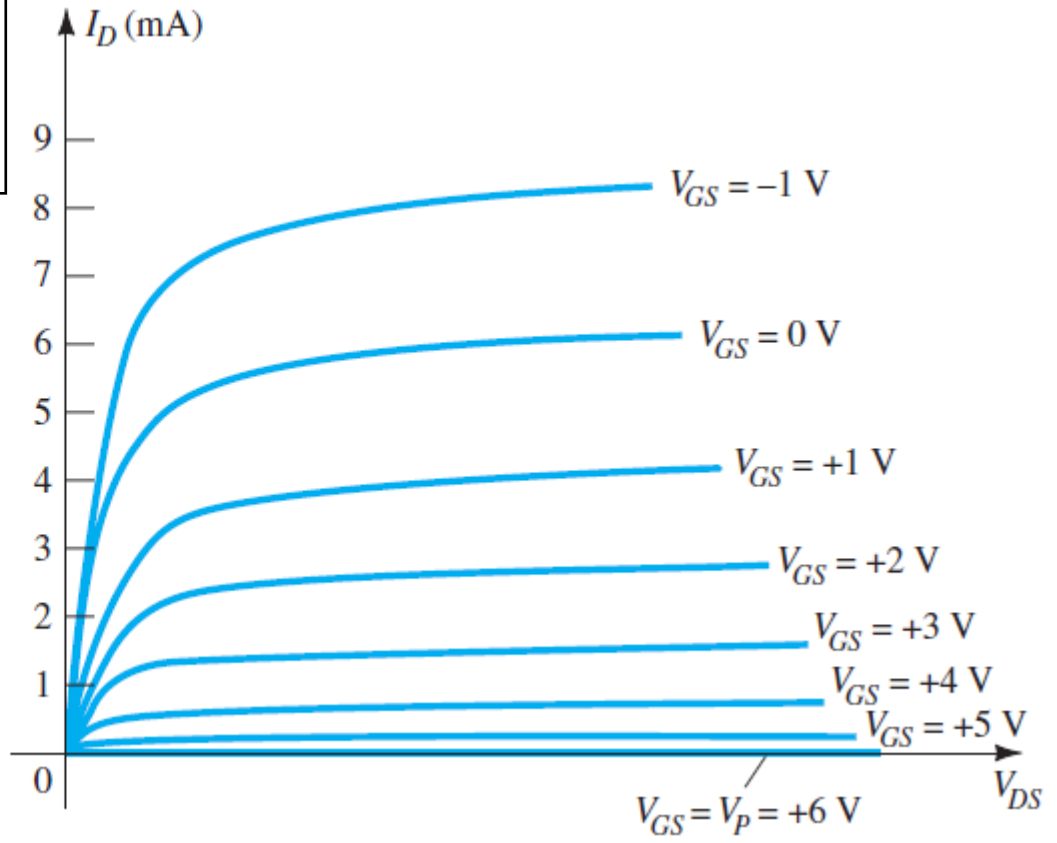
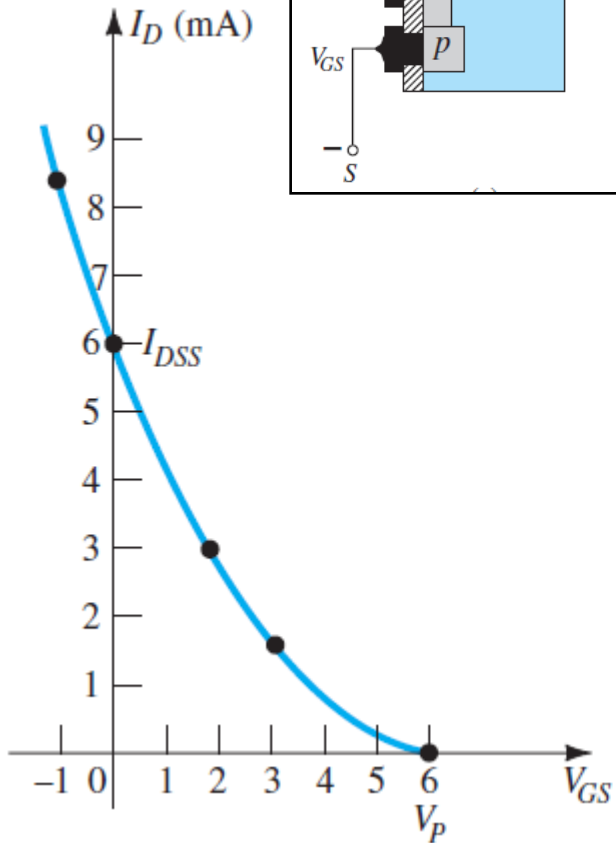
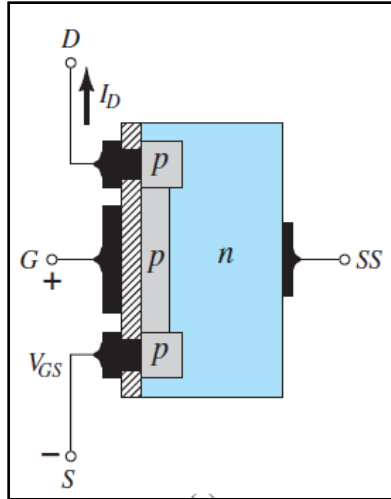
# Basic Operation and Characteristics n-Channel Depletion-type MOSFETS

Drain and transfer characteristics for an n-channel depletion-type MOSFET.

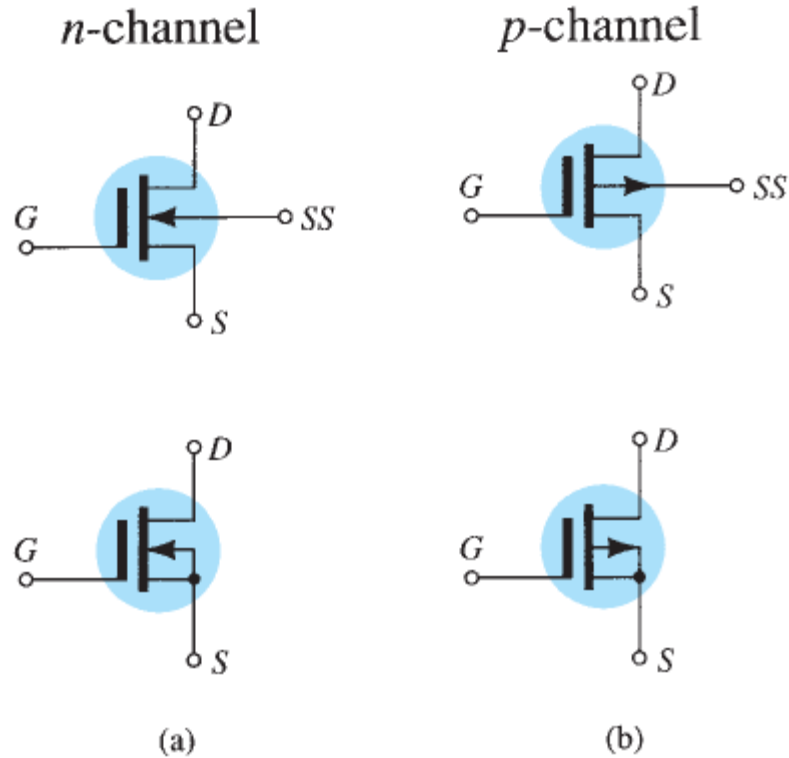


- ❑ Application of a positive gate-to-source voltage has “enhanced” the level of free carriers in the channel compared to that encountered with  $V_{GS} = 0$
- ❑ For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement* region, with the region between cutoff and the saturation level of  $I_{DSS}$  referred to as the *depletion* region.

# p -Channel Depletion-Type MOSFET



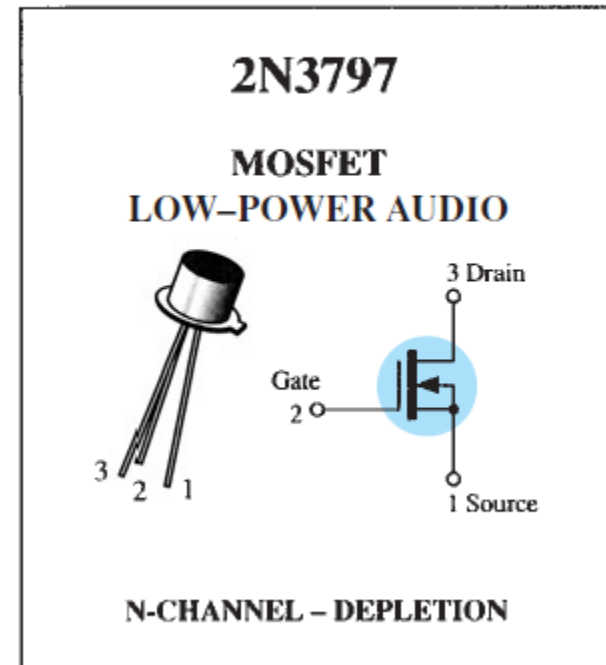
# Depletion-Type MOSFET Symbols



# MOSFET Specification Sheet

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage 2N3797	$V_{DS}$	20	Vdc
Gate-Source Voltage	$V_{GS}$	$\pm 10$	Vdc
Drain Current	$I_D$	20	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	200 1.14	mW mW/ $^\circ\text{C}$
Junction Temperature Range	$T_J$	+175	$^\circ\text{C}$
Storage Channel Temperature Range	$T_{stg}$	-65 to +200	$^\circ\text{C}$



# MOSFET Specification Sheet

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain Source Breakdown Voltage ( $V_{GS} = -7.0\text{ V}$ , $I_D = 5.0\ \mu\text{A}$ )	$V_{(BR)DSX}$	20	25	–	Vdc
Gate Reverse Current (1) ( $V_{GS} = -10\text{ V}$ , $V_{DS} = 0$ ) ( $V_{GS} = -10\text{ V}$ , $V_{DS} = 0$ , $T_A = 150^\circ\text{C}$ )	$I_{GSS}$	–	–	1.0 200	pAde
Gate Source Cutoff Voltage ( $I_D = 2.0\ \mu\text{A}$ , $V_{DS} = 10\text{ V}$ )	$V_{GS(off)}$	–	–5.0	–7.0	Vdc
Drain-Gate Reverse Current (1) ( $V_{DG} = 10\text{ V}$ , $I_S = 0$ )	$I_{DGO}$	–	–	1.0	pAde
<b>ON CHARACTERISTICS</b>					
Zero-Gate-Voltage Drain Current ( $V_{DS} = 10\text{ V}$ , $V_{GS} = 0$ )	$I_{DSS}$	2.0	2.9	6.0	mAdc
On-State Drain Current ( $V_{DS} = 10\text{ V}$ , $V_{GS} = +3.5\text{ V}$ )	$I_{D(on)}$	9.0	14	18	mAdc

# MOSFET Specification Sheet

## SMALL-SIGNAL CHARACTERISTICS

Forward Transfer Admittance ( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ )	2N3797	$ Y_{fs} $	1500	2300	3000	$\mu\text{mhos}$
( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1.0 \text{ MHz}$ )	2N3797		1500	–	–	
Output Admittance ( $I_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ )	2N3797	$ Y_{os} $	–	27	60	$\mu\text{mhos}$
Input Capacitance ( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1.0 \text{ MHz}$ )	2N3797	$C_{iss}$	–	6.0	8.0	pF
Reverse Transfer Capacitance ( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1.0 \text{ MHz}$ )		$C_{rss}$	–	0.5	0.8	pF

## FUNCTIONAL CHARACTERISTICS

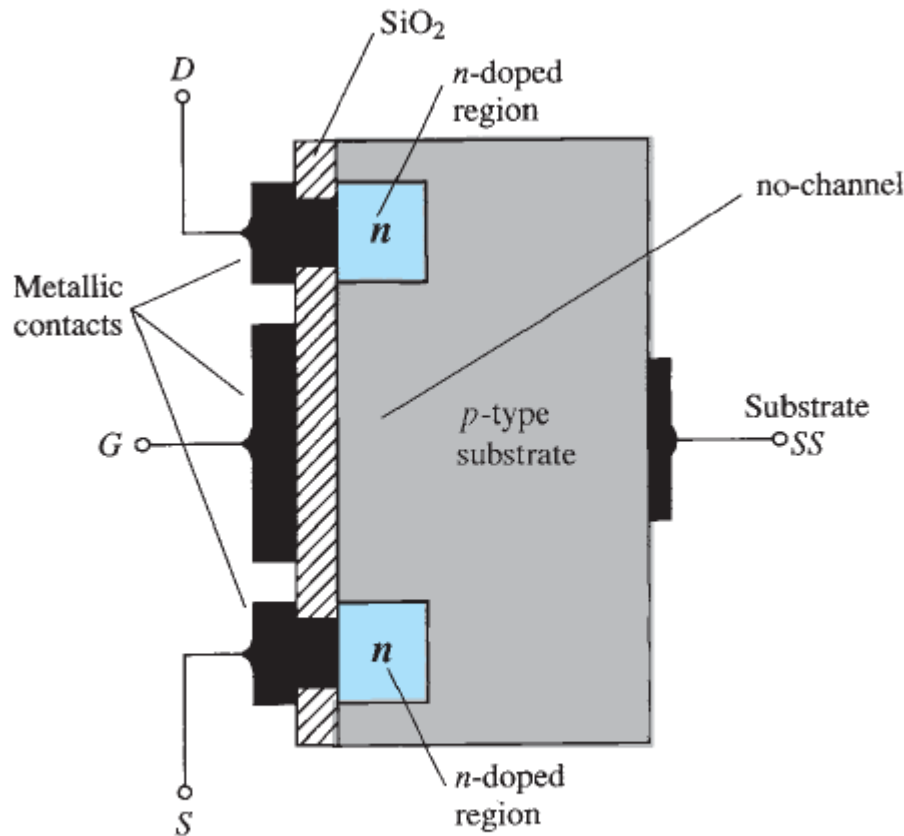
Noise Figure ( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 1.0 \text{ kHz}$ , $R_S = 3 \text{ megohms}$ )		NF	–	3.8	–	dB
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(1) This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.

# Enhancement -Type MOSFET

- ❑ There are some similarities in construction and mode of operation between depletion type and enhancement-type MOSFETs.
- ❑ But, the characteristics of the enhancement-type MOSFET are quite different from anything obtained thus far.
- ❑ The transfer curve is not defined by Shockley's equation, and the drain current is now cut off until the gate-to source voltage reaches a specific magnitude.

# Structure of n-Channel Enhancement -Type MOSFET

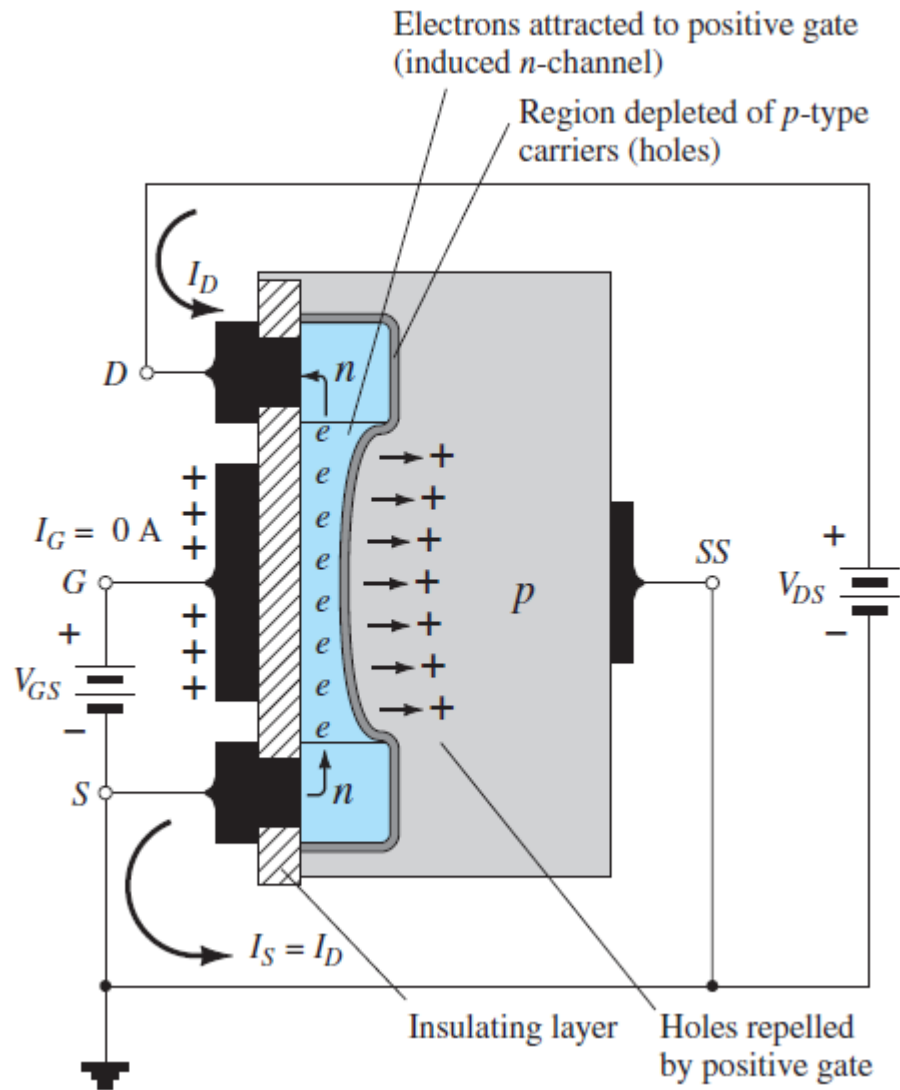


**FIG. 6.32**

*n-Channel enhancement-type MOSFET.*

- ❑ A slab of p -type material is formed from a silicon base and is again referred to as the substrate.
- ❑ As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal.
- ❑ The source and drain terminals are again connected through metallic contacts to n-doped regions.
- ❑ But note the absence of a channel between the two n -doped regions.
- ❑ The SiO<sub>2</sub> layer is still present to isolate the gate metallic platform from the region between the drain and source.
- ❑ If  $V_{GS} = 0V$  and  $V_{DS} > 0V$  the absence of an n-channel will result in a current of effectively 0A (quite different from the depletion-type MOSFET and JFET)

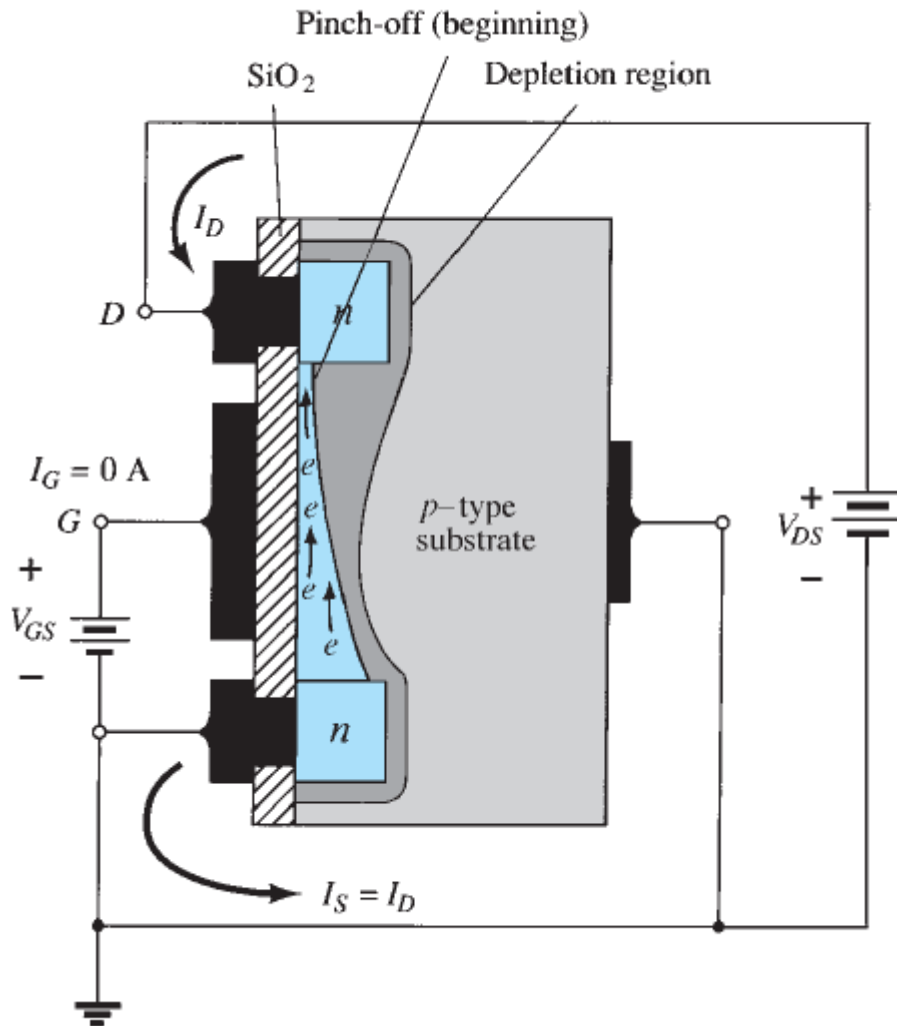
# Structure of n-Channel Enhancement -Type MOSFET



- with  $V_{GS} > 0$  and  $V_{DS} > 0$  establishing the drain and the gate at a positive potential with respect to the source:
- ❑ Positive potential at the gate will pressure the holes in the  $p$ -substrate along the edge of the  $\text{SiO}_2$  to enter deeper into the  $p$ -substrate.
  - ❑ Resulting in a depletion region near the  $\text{SiO}_2$  insulating layer void of holes.
  - ❑ However, the electrons in the  $p$ -substrate will be attracted to the positive gate and accumulate in the at the surface of the  $\text{SiO}_2$  layer.
  - ❑ The  $\text{SiO}_2$  layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal.
  - ❑ Once  $V_{GS}$  is large enough the induced n-type region can support a measurable current.



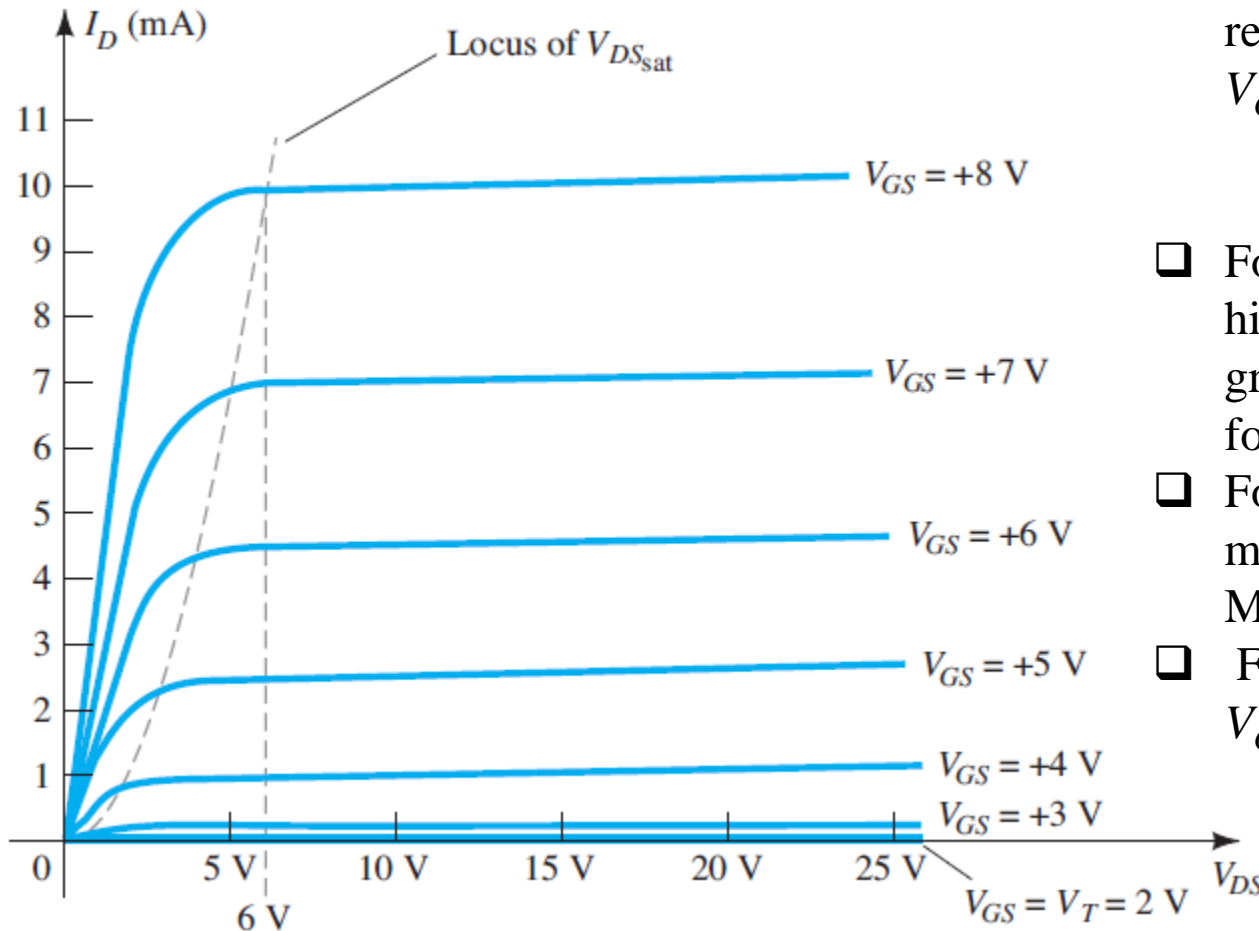
# Structure of n-Channel Enhancement -Type MOSFET



- ❑ If we hold  $V_{GS}$  constant and increase the level of  $V_{DS}$ , the drain current will eventually reach a saturation level.
- ❑ This reduction in gate-to-drain voltage results in the condition  $V_{GD} < V_t$  which means that the channel no longer exists at the drain[1].
- ❑ Causing a reduction in the effective channel width.
- ❑ Eventually, the channel will be reduced to the point of pinch-off and resulting in saturation.
- ❑ The levelling off of  $I_D$  is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel.

[1] Analysis and design of Analog Integrated Circuits 4e, Hurst and Meyer

# Drain characteristics of an *n*-channel enhancement-type MOSFET



- The saturation level for  $V_{DS}$  is related to the level of applied  $V_{GS}$  by:

$$V_{DS_{sat}} = V_{GS} - V_T$$

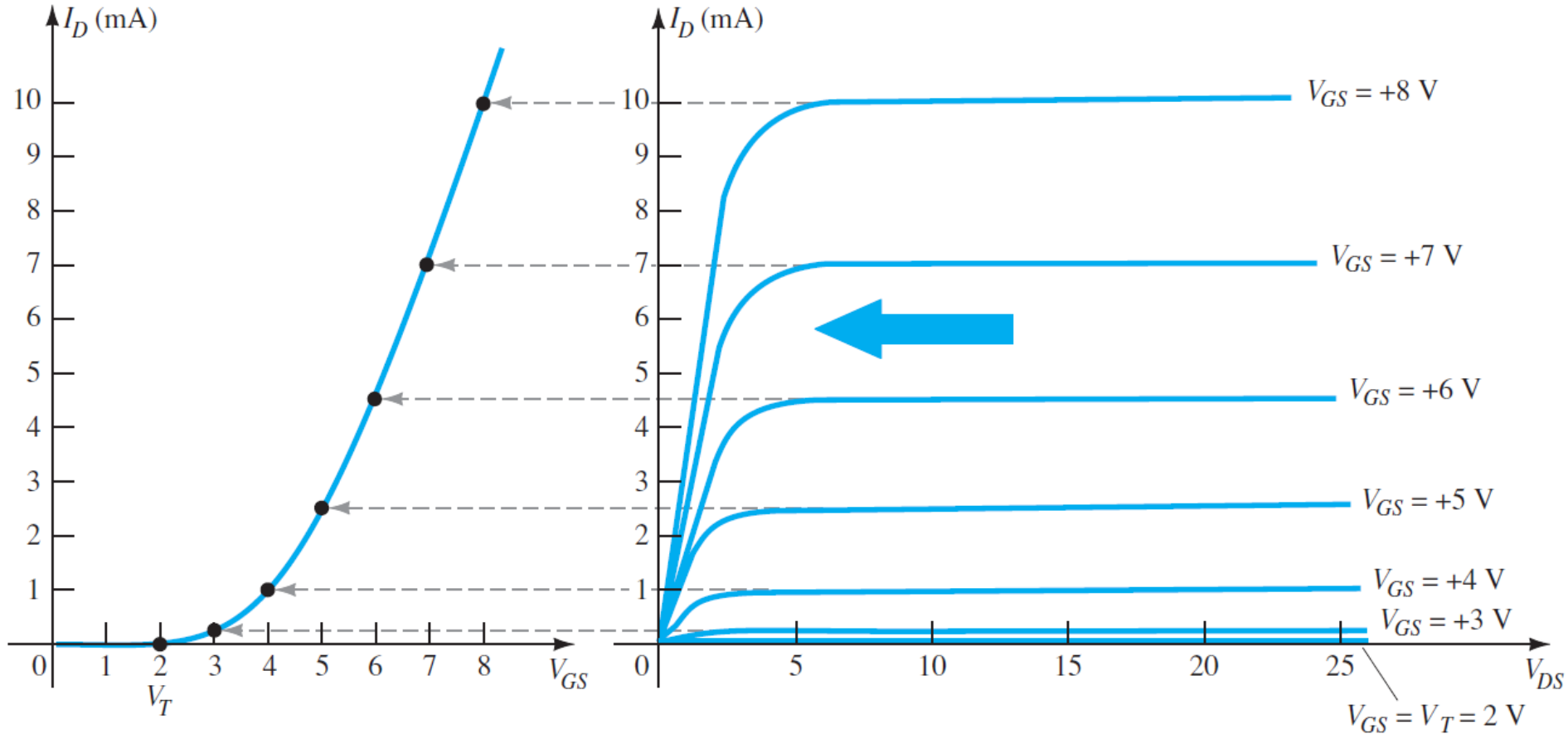
- For a fixed value of  $V_T$ , the higher the level of  $V_{GS}$ , the greater is the saturation level for  $V_{DS}$ .
- For values of  $V_{GS} < V_T$ ,  $I_D = 0$  mA for enhancement type MOSFET.
- For  $V_{GS} > V_T$ ,  $I_D$  is related to  $V_{GS}$  by:

$$I_D = k(V_{GS} - V_T)^2$$

Where:

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

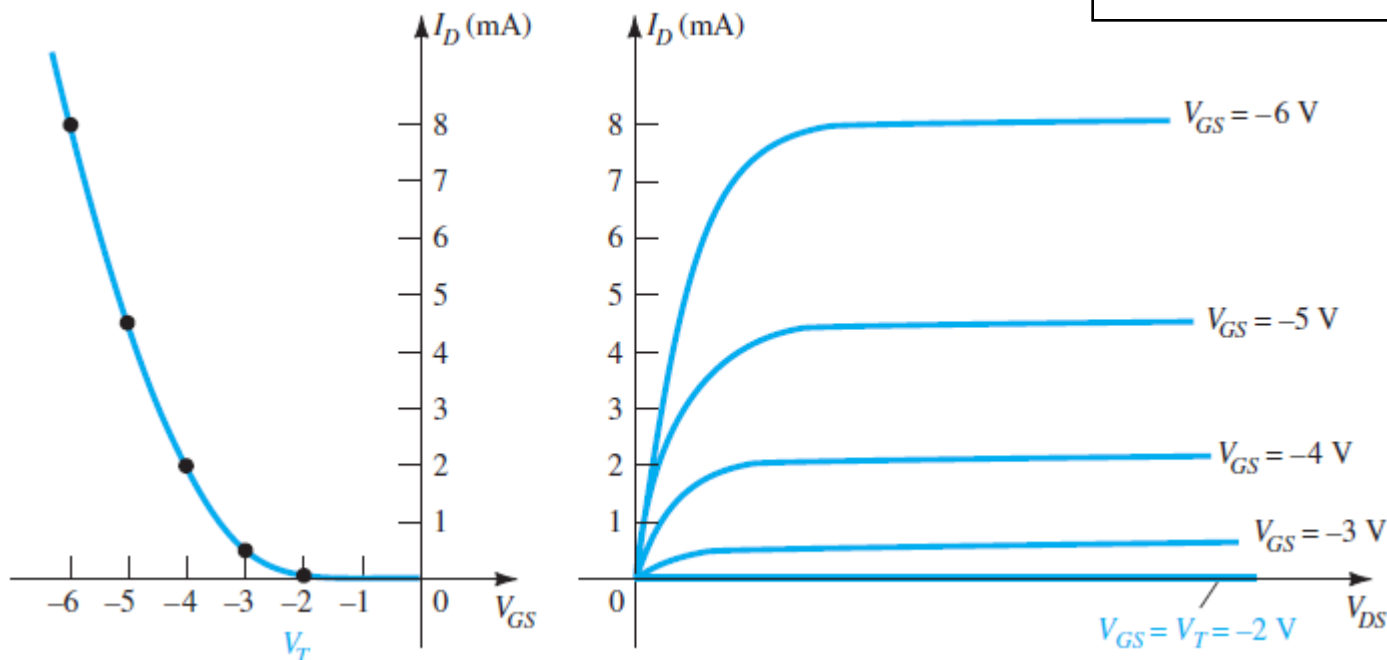
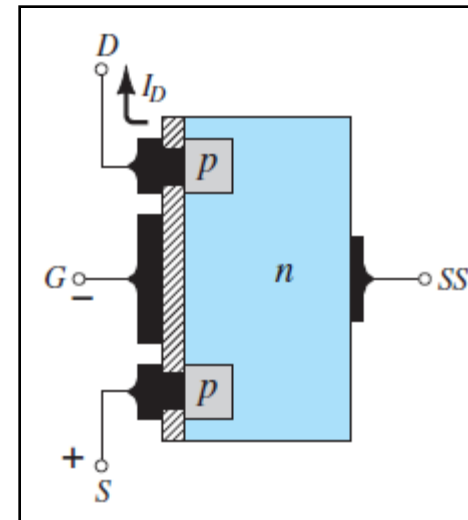
# Sketching the transfer characteristics for an n-channel enhancement-type MOSFET from the drain characteristics



- For the dc analysis of enhancement-type MOSFETs, the transfer characteristics will again be the characteristics to be employed in the graphical solution.

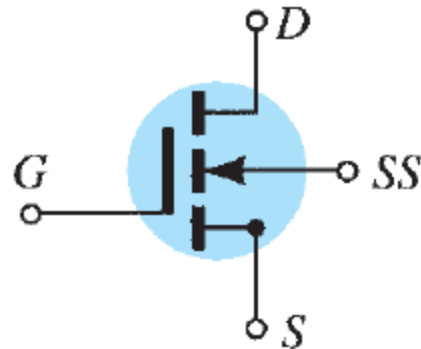
# p -Channel Enhancement-Type MOSFETs

- ❑ The construction of a  $p$ -channel enhancement-type MOSFET is exactly the reverse of the  $n$ -Channel variant.
- ❑ The terminals remain as identified, but all the voltage polarities and the current directions are reversed

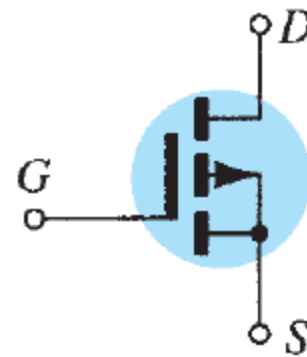
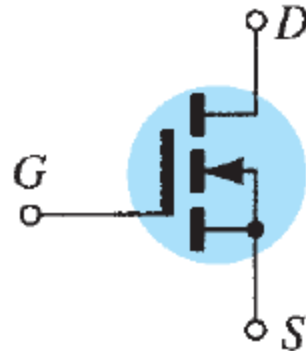
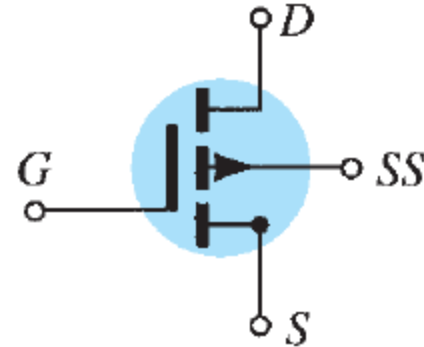


# Symbols for $n$ and $p$ -channel enhancement-type MOSFETs

$n$ -channel



$p$ -channel



# 2N4351 Motorola n-channel enhancement-type MOSFET

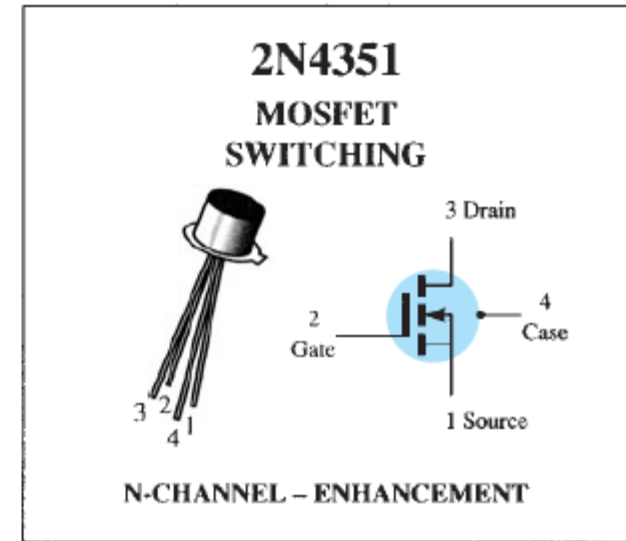
## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	25	Vdc
Drain-Gate Voltage	$V_{DG}$	30	Vdc
Gate-Source Voltage*	$V_{GS}$	30	Vdc
Drain Current	$I_D$	30	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300 1.7	mW mW/ $^\circ\text{C}$
Junction Temperature Range	$T_J$	175	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-65 to +175	$^\circ\text{C}$

\* Transient potentials of  $\pm 75$  Volt will not cause gate-oxide failure.

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Drain-Source Breakdown Voltage ( $I_D = 10 \mu\text{A}$ , $V_{GS} = 0$ )	$V_{(BR)DSX}$	25	-	Vdc
Zero-Gate-Voltage Drain Current ( $V_{DS} = 10 \text{V}$ , $V_{GS} = 0$ )	$I_{DSS}$	$T_A = 25^\circ\text{C}$	10	nAdc
		$T_A = 150^\circ\text{C}$	10	$\mu\text{Adc}$
Gate Reverse Current ( $V_{GS} = \pm 15 \text{Vdc}$ , $V_{DS} = 0$ )	$I_{GSS}$	-	$\pm 10$	pAdc



# 2N4351 Motorola n-channel enhancement-type MOSFET

## ON CHARACTERISTICS

Gate Threshold Voltage ( $V_{DS} = 10 \text{ V}$ , $I_D = 10 \mu\text{A}$ )	$V_{GS(Th)}$	1.0	5	Vdc
Drain-Source On-Voltage ( $I_D = 2.0 \text{ mA}$ , $V_{GS} = 10\text{V}$ )	$V_{DS(on)}$	–	1.0	V
On-State Drain Current ( $V_{GS} = 10 \text{ V}$ , $V_{DS} = 10 \text{ V}$ )	$I_{D(on)}$	3.0	–	mAdc

## SMALL-SIGNAL CHARACTERISTICS

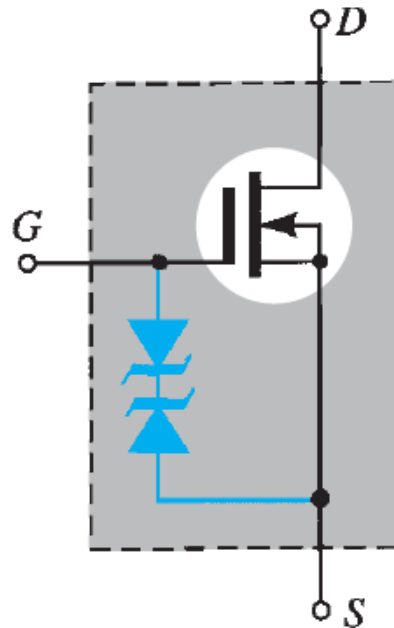
Forward Transfer Admittance ( $V_{DS} = 10 \text{ V}$ , $I_D = 2.0 \text{ mA}$ , $f = 1.0 \text{ kHz}$ )	$ y_{fs} $	1000	–	$\mu\text{mho}$
Input Capacitance ( $V_{DS} = 10 \text{ V}$ , $V_{GS} = 0$ , $f = 140 \text{ kHz}$ )	$C_{iss}$	–	5.0	pF
Reverse Transfer Capacitance ( $V_{DS} = 0$ , $V_{GS} = 0$ , $f = 140 \text{ kHz}$ )	$C_{rss}$	–	1.3	pF
Drain-Substrate Capacitance ( $V_{D(SUB)} = 10 \text{ V}$ , $f = 140 \text{ kHz}$ )	$C_{d(sub)}$	–	5.0	pF
Drain-Source Resistance ( $V_{GS} = 10 \text{ V}$ , $I_D = 0$ , $f = 1.0 \text{ kHz}$ )	$r_{ds(on)}$	–	300	ohms

## SWITCHING CHARACTERISTICS

Turn-On Delay (Fig. 5)	$I_D = 2.0 \text{ mAdc}$ , $V_{DS} = 10 \text{ Vdc}$ , ( $V_{GS} = 10 \text{ Vdc}$ ) (See Figure 9; Times Circuit Determined)	$t_{d1}$	–	45	ns
Rise Time (Fig. 6)		$t_r$	–	65	ns
Turn-Off Delay (Fig. 7)		$t_{d2}$	–	60	ns
Fall Time (Fig. 8)		$t_f$	–	100	ns

# MOSFET HANDLING

- ❑ The thin  $\text{SiO}_2$  layer between the gate and the channel of MOSFETs has the positive effect of providing a high-input-impedance characteristic for the device, but because of its extremely thin layer, it introduces a concern for its handling that was not present for the BJT or JFET transistors.

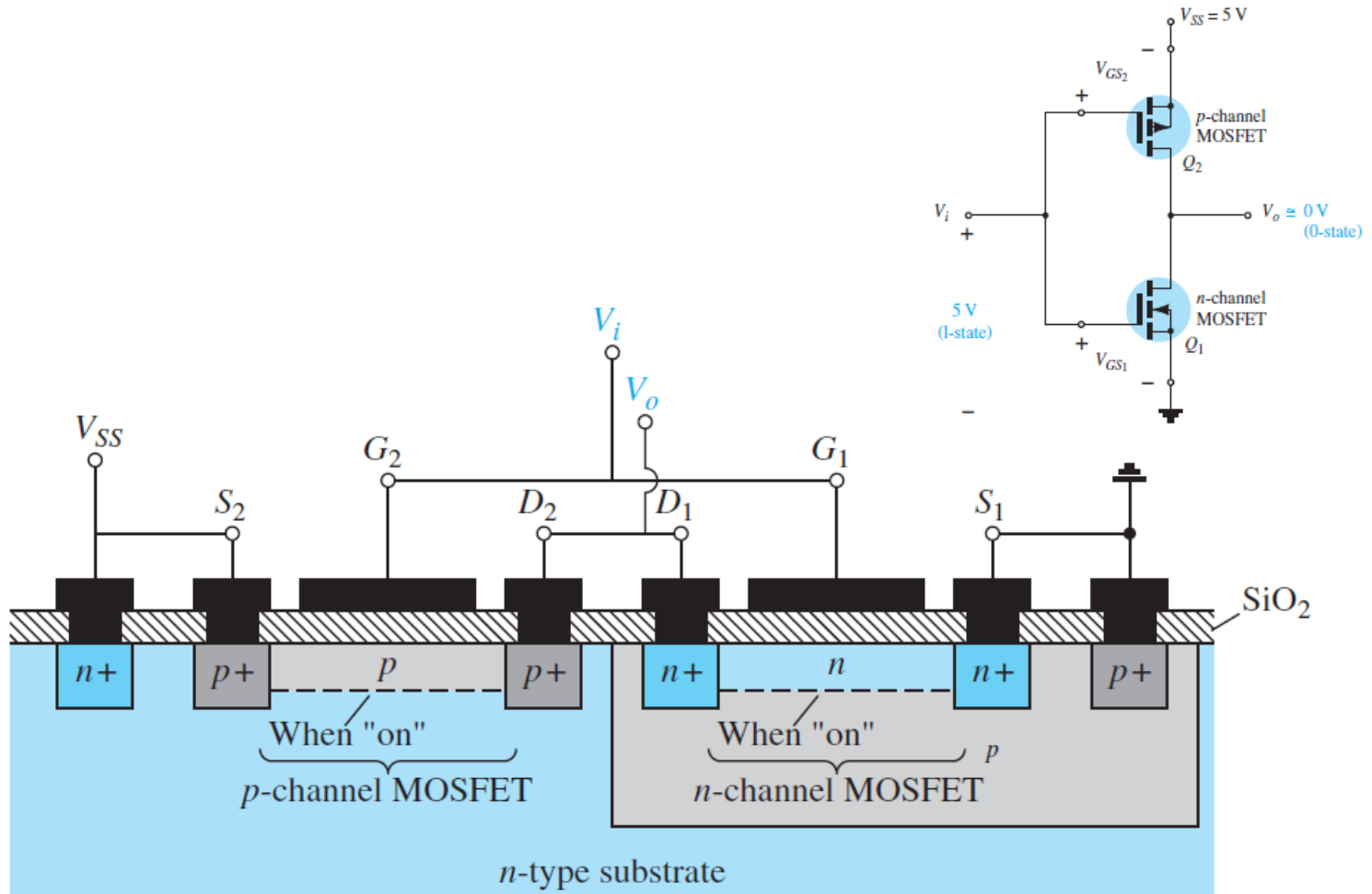


**FIG. 6.42**

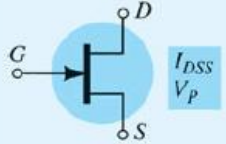
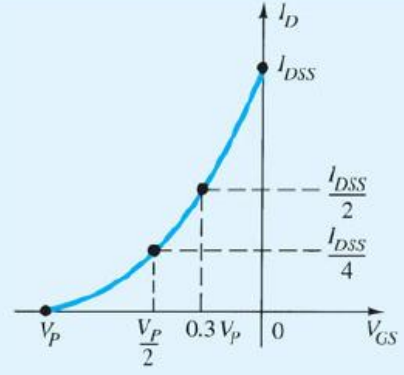

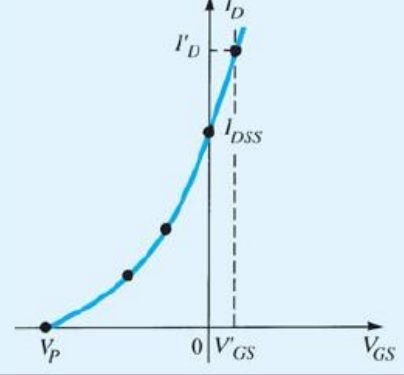
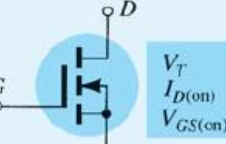
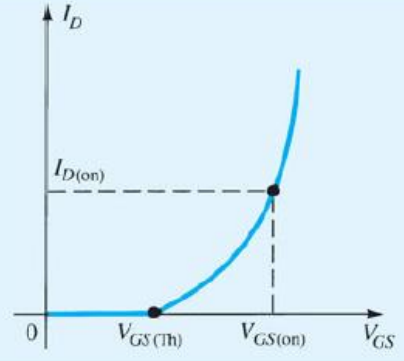
*Zener-protected MOSFET.*

# complementary MOSFET (CMOS)

- A very effective logic circuit can be established by constructing a  $p$ -channel and an  $n$ -channel MOSFET on the same substrate. E.g CMOS NOT gate (inverter)



# JFET and MOSFETs

Type	Symbol and Basic Relationships	Transfer Curve	Input Resistance and Capacitance
JFET (n-channel)	$I_G = 0 \text{ A}, I_D = I_S$  $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 100 \text{ M}\Omega$ $C_i: (1 - 10) \text{ pF}$
MOSFET depletion type (n-channel)	$I_G = 0 \text{ A}, I_D = I_S$  $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 10^{10} \Omega$ $C_i: (1 - 10) \text{ pF}$
MOSFET enhancement type (n-channel)	$I_G = 0 \text{ A}, I_D = I_S$  $I_D = k (V_{GS} - V_{GS(Th)})^2$ $k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$		$R_i > 10^{10} \Omega$ $C_i: (1 - 10) \text{ pF}$

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# End of Lecture 6

*Thank you for your attention!*